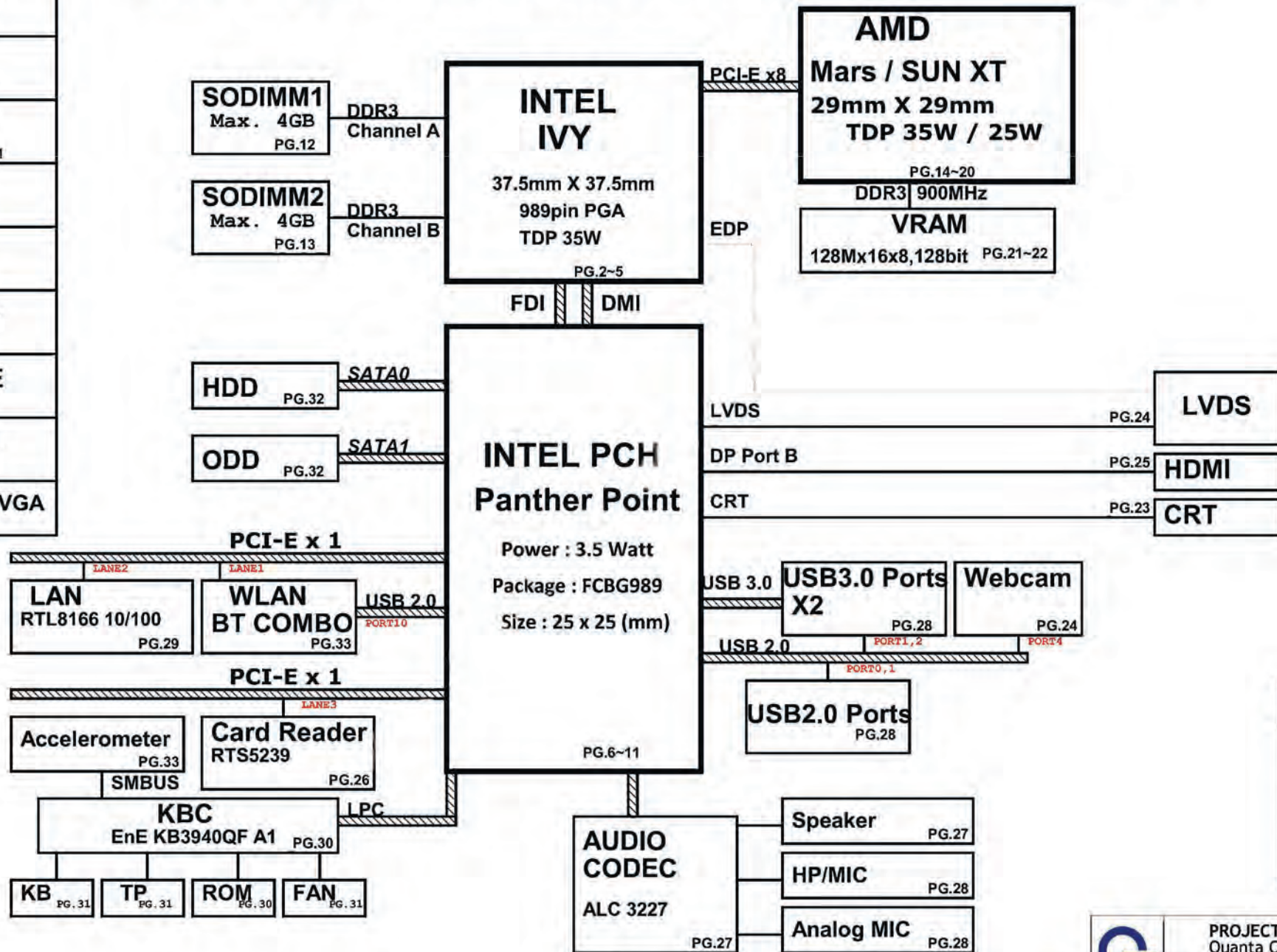
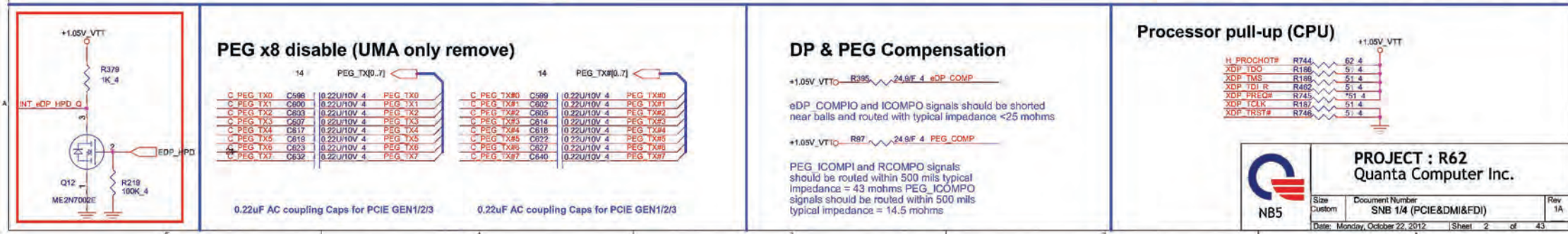
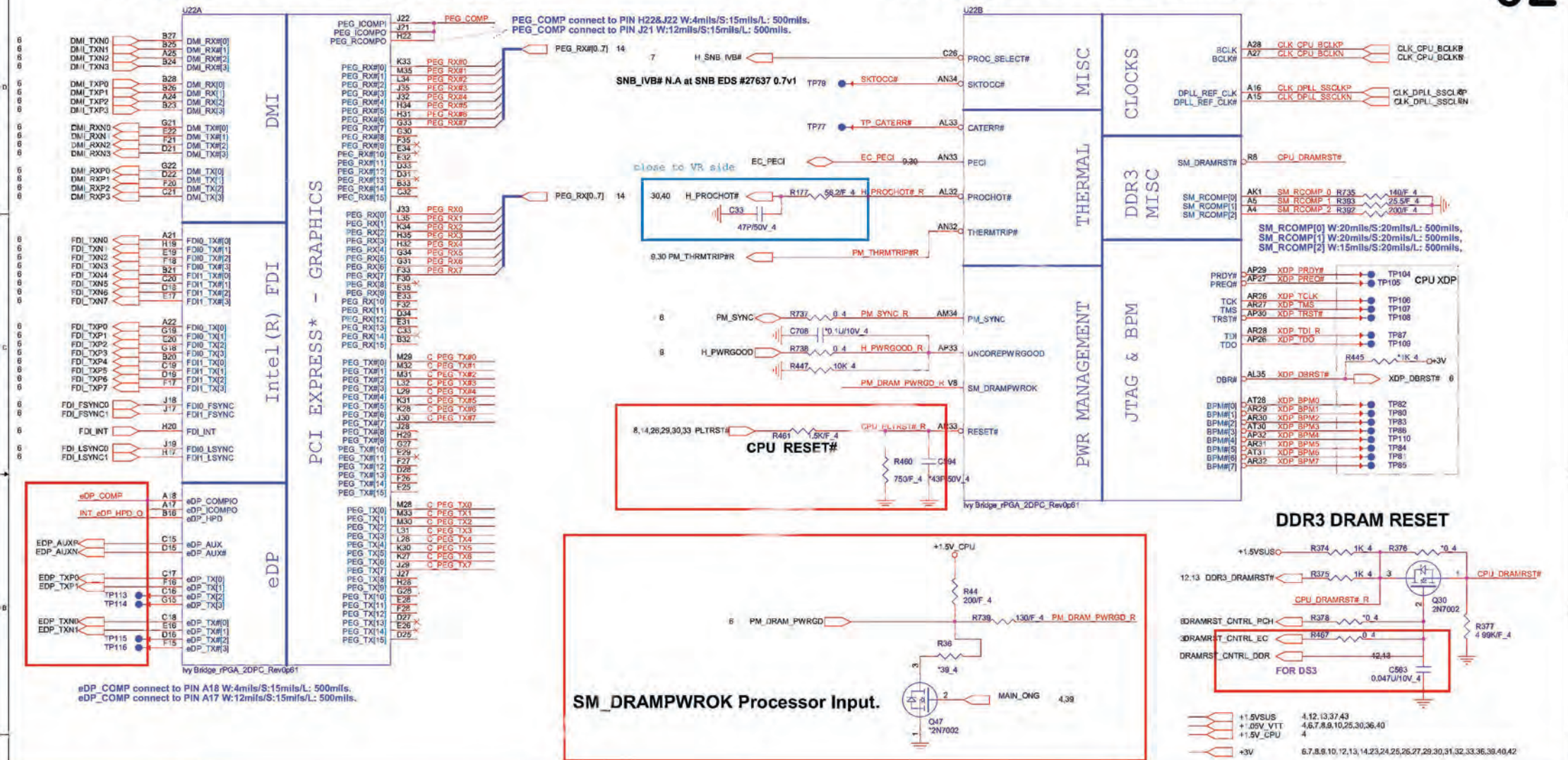


|                           |
|---------------------------|
| <b>+3V/+5V S5</b>         |
| PG.35                     |
| <b>+1.05V</b>             |
| PG.36                     |
| <b>CPU Core</b>           |
| PG.40~41                  |
| <b>DDR3</b>               |
| PG.37                     |
| <b>Charge</b>             |
| PG.34                     |
| <b>Dis-Charge</b>         |
| PG.39                     |
| <b>+VGACORE</b>           |
| PG.42                     |
| <b>+VCCSA</b>             |
| PG.38                     |
| <b>+1.0V/+1.8/ +3 VGA</b> |
| PG.43                     |

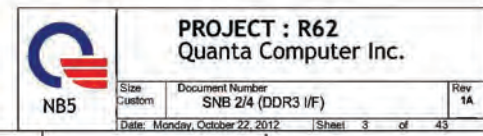








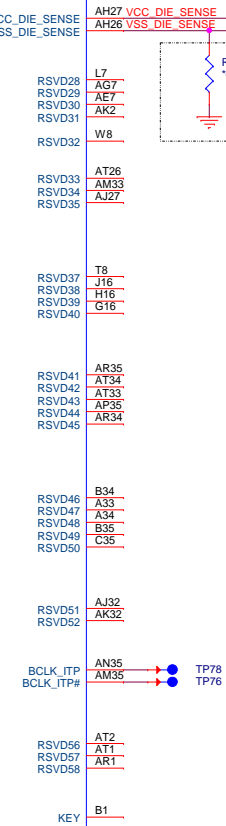
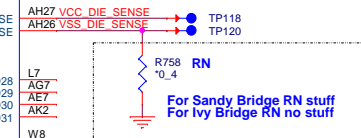
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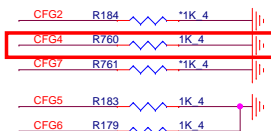


## POWER





For rPGA socket, RSVD59 pin should be left NC.

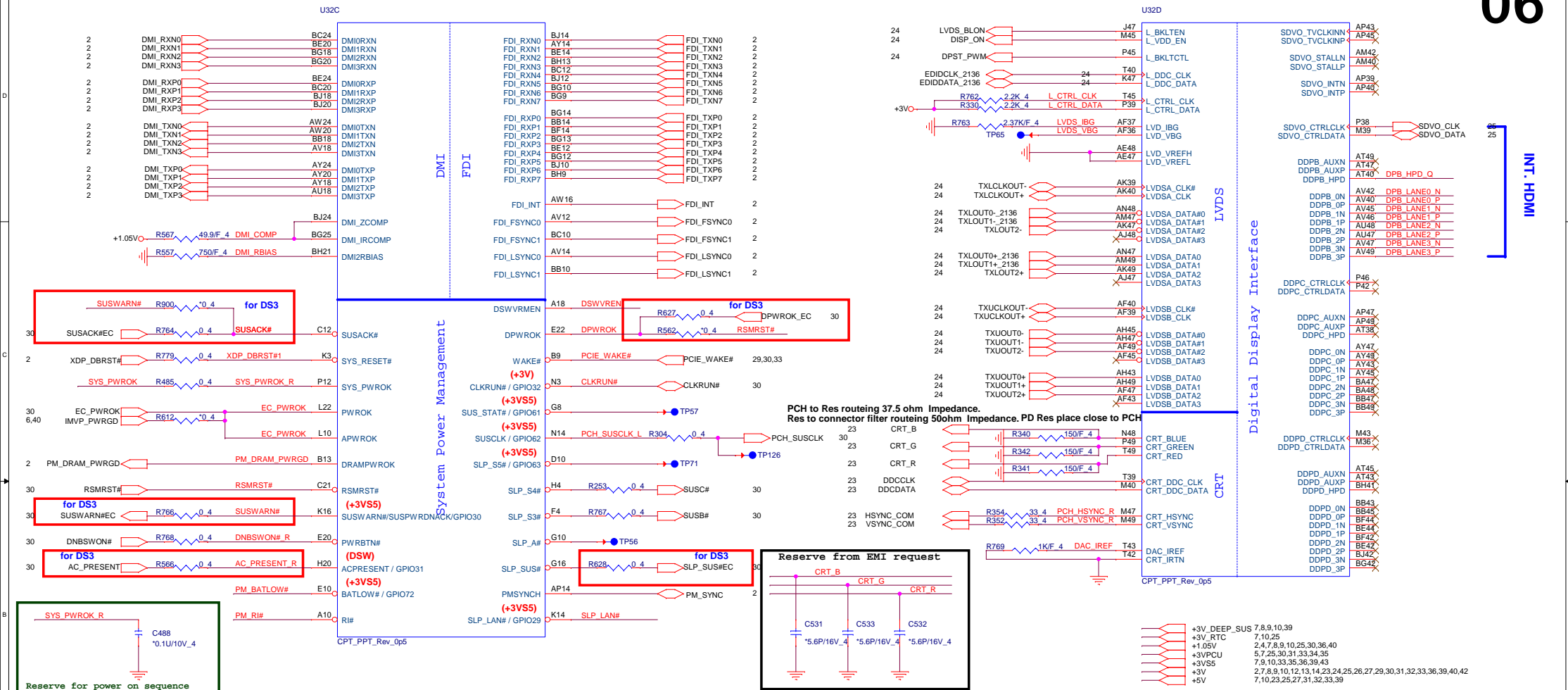


```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```








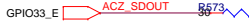
The CFG signals have a default value of '1' if not terminated on the board.

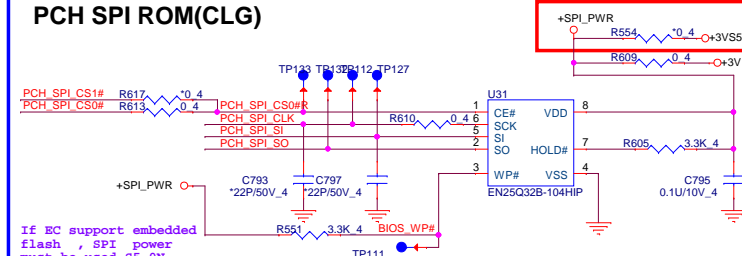
|                                    | 1  | 0  |
|------------------------------------|--|--|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation   | Lane Reversed                                |
| CFG4<br>(DP Presence Strap)        | Disable; No physical DP attached to eDP                  | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training)       | PEG train immediately following<br>xxRESETB de assertion | PEG wait for BIOS training                   |







| Pin Name                                     | Strap description                                      | Sampled       | Configuration   | Circuit  |       |               |   |   |            |  |
|--|--|---------------|---|--|-------|---------------|---|---|------------|--|
| SPKR<br><div>Different from Calpella</div>   | No reboot mode setting                                 | PWROK         | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode   |  |       |               |   |   |            |  |
| GNT3# / GPIO55                               | Top-Block Swap Override                                | PWROK         | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K)   | +3V <sub>0</sub>  PCI_GNT3# 8  |       |               |   |   |            |  |
| INTVRMEN                                     | Integrated 1.05V VRM enable                            | ALWAYS        | Should be always pull-up  |  +3V_RTC   |       |               |   |   |            |  |
| HDA_DOCK_EN#/GPIO33                          | Flash Descriptor Security<br>Only for Interposer       | PWROK         | 0 = Override<br>1 = Default (weak pull-up 20K)  |  BIOS_WP#  |       |               |   |   |            |  |
| GNT1# / GPIO51                               | Boot BIOS Selection 1 [bit-1]                          | PWROK         | <table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>0</td><td>SPI<br/>LPC</td></tr></table> | GNT1#  | GNT0# | Boot Location | 1 | 0 | SPI<br>LPC | [Need external pull-down for LPC BIOS]<br>Default weak pull-up on GNT0/1#<br> BBS_BIT0<br>BBS_BIT1 8 |
| GNT1#  | GNT0#  | Boot Location |   |  |       |               |   |   |            |  |
| 1  | 0  | SPI<br>LPC    |   |  |       |               |   |   |            |  |
| GPIO19<br><div>Different from Calpella</div> | Boot BIOS Selection 0 [bit-0]                          | PWROK         |   |  |       |               |   |   |            |  |
| GNT2# / GPIO53                               | ESI strap (Server only)                                | PWROK         | Should not be pull-down<br>(weak pull-up 20K)   | USE GPIO PIN   |       |               |   |   |            |  |
| NV_ALE                                       | Intel Anti-Theft HDD protection<br>Only for Interposer | PWROK         | 0 = Disable (Internal pull-down 20kohm)   | +1.8V <sub>0</sub>  NV_ALE 8   |       |               |   |   |            |  |
| NV_CLE                                       | DMI Termination voltage                                | PWROK         | weak pull-down 20kohm   | +1.8V <sub>0</sub>  NV_CLE 9<br>H_SNB_IVB# 2<br><i>Sandy / Ivy / Ivy</i> |       |               |   |   |            |  |
| HDA_SYNC                                     | On-Die PLL VR Voltage Select                           | RSMRST        | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V   |  +V3.3A_1.5A_HDA_IO ACZ_SYNC   |       |               |   |   |            |  |
| HDA_SDO                                      | Flash Descriptor Security                              | PWROK         | 0 = Default (weak pull-down 20K)<br>1 = Overridden  | GPIO33_E  +V3.3A_1.5A_HDA_IO   |       |               |   |   |            |  |
| GPIO8  | Integrated Clock Chip Enable                           | RSMRST#       | Should be pull-down (weak pull-up 20K)  |  |       |               |   |   |            |  |
| GPIO28<br><div>Different from Calpella</div> | On-die PLL Voltage Regulator                           | RSMRST#       | 0 = Disable<br>1 = Enable (Default)   |  |       |               |   |   |            |  |
| SPI_MOSI                                     | iTPM function Disable                                  | APWROK        | 0 = Default (weak pull-down 20K)<br>1 = Enable  |  |       |               |   |   |            |  |



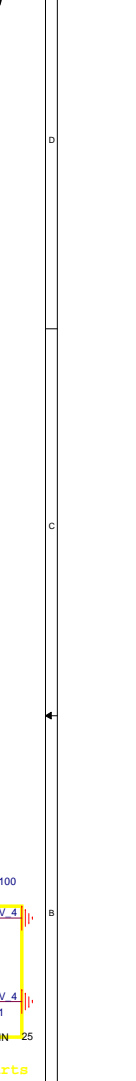
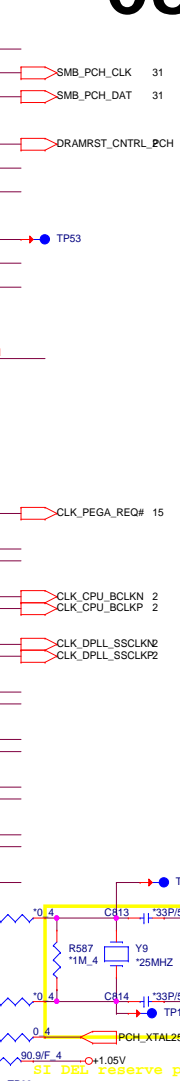
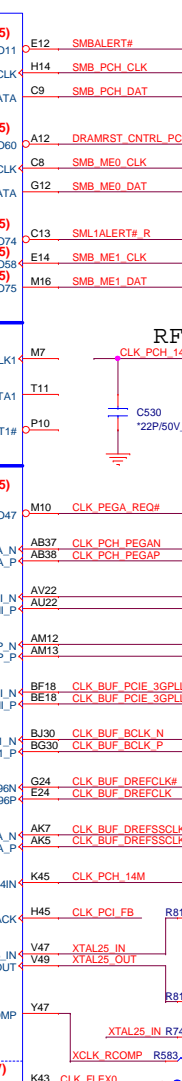
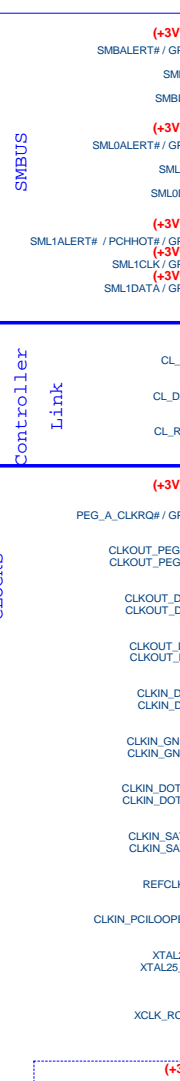
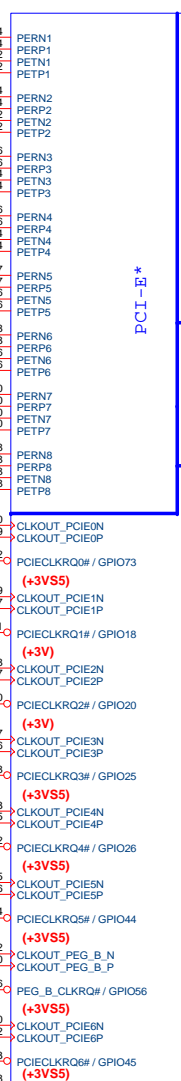
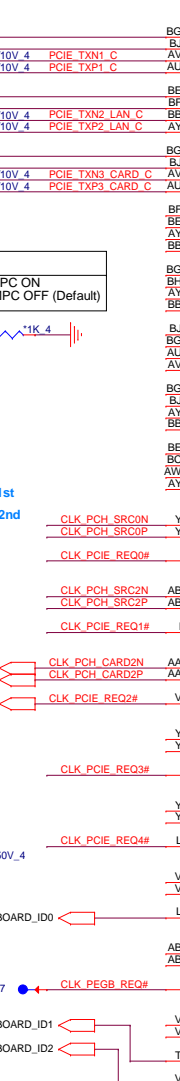
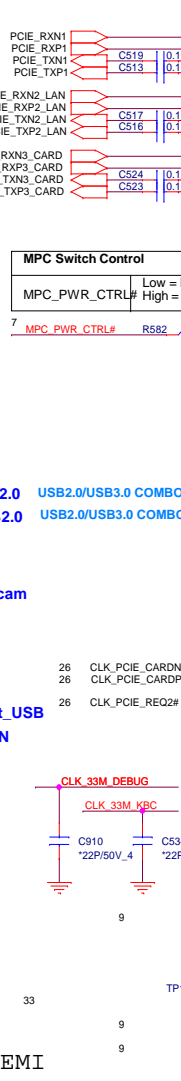
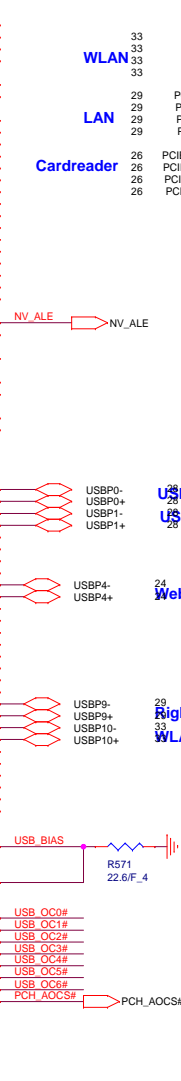
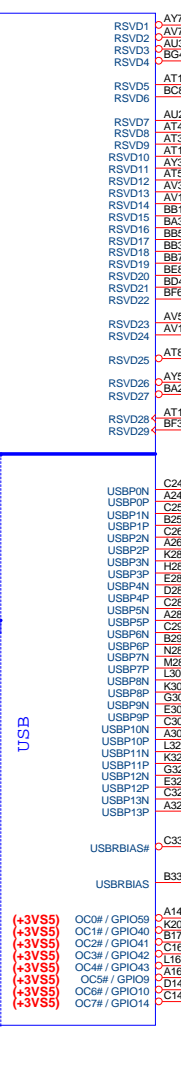
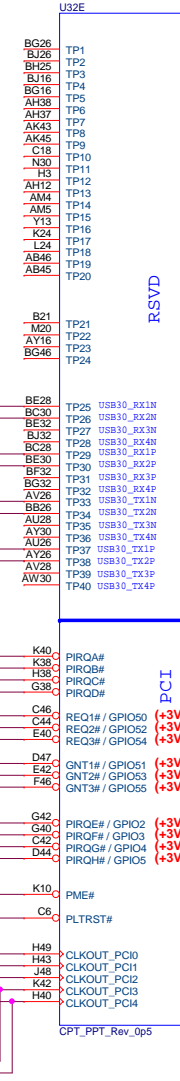
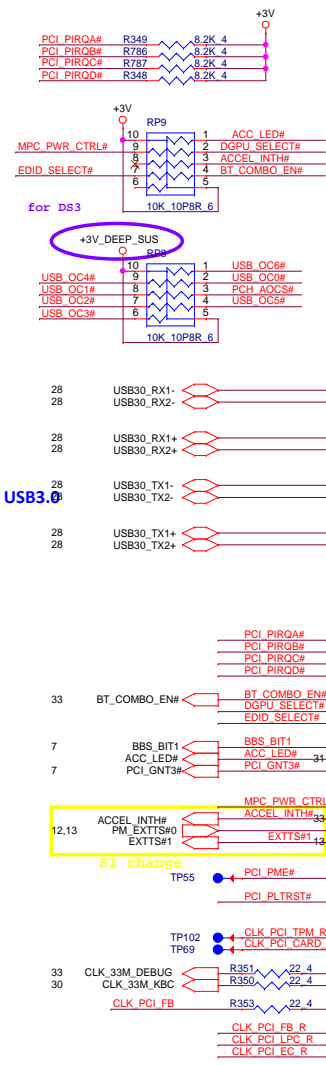
| Vender | Size | P/N                           |
|--------|------|-------------------------------|
| EON    | 4MB  | AKE39ZN0Q02 (EN25Q32B-104HIP) |
| PMC    | 4MB  | AKE39ZN0500 (PM25LQ032C-BCE)  |
| AMIC   | 4MB  | AKE39F-0800 (A25LQ32AM-F/Q)   |
| Socket |      | DFHS08FS023                   |



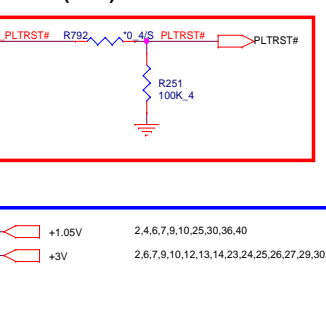
**PROJECT : R62**  
Quanta Computer Inc.

|                                |   |               |
|--------------------------------|---|---------------|
| Size<br>Custom                 | Document Number<br>PCH 2/6 (SATA/HDA/SPI) | Rev<br>1A     |
| Date: Monday, October 22, 2012 |   | Sheet 7 of 43 |

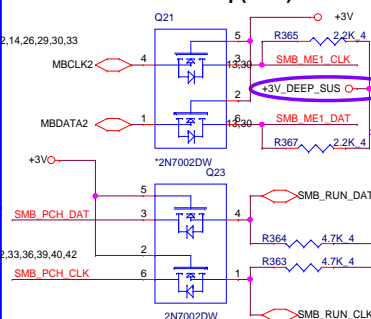
PCI/USB/OC# Pull-up(CLG)



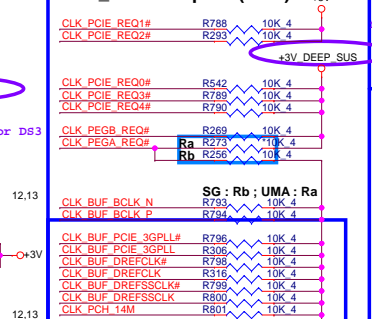
PLTRST#(CLG)



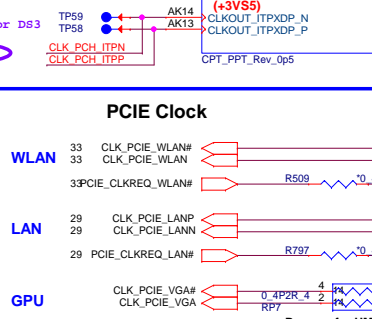
SMBus/Pull-up(CLG)



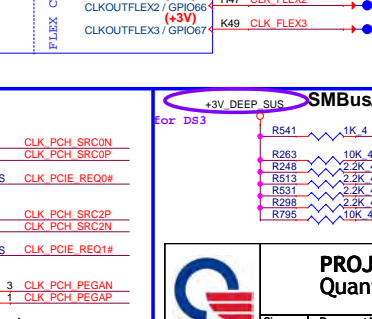
CLK\_REQ/Strap Pin(CLG)



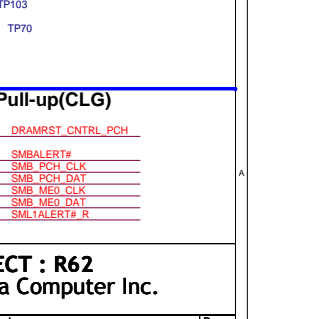
PCIE Clock



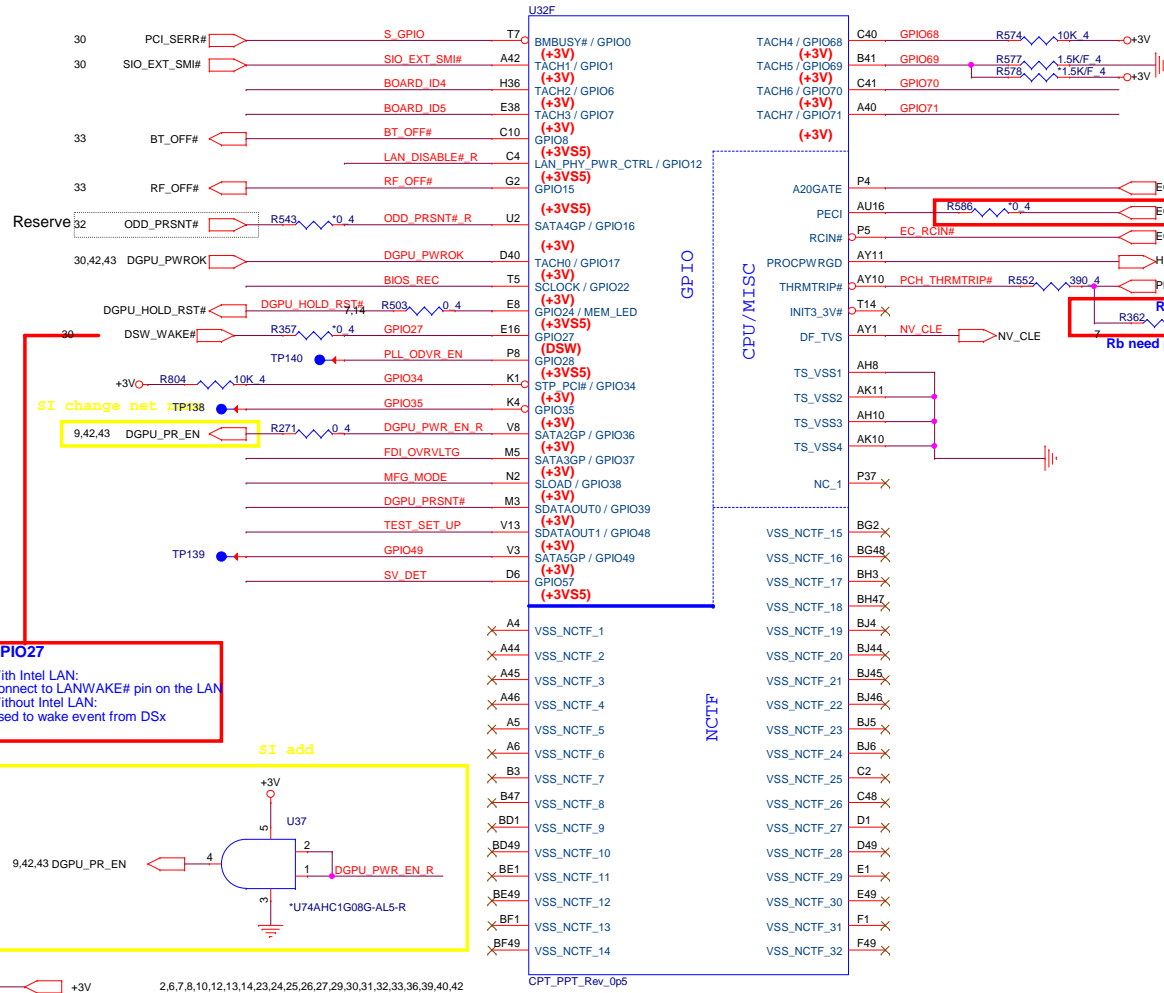
WLAN



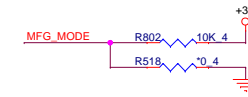
LAN





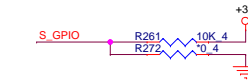


### MFG-TEST

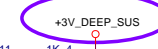


### Swap GPIO

0 = SGPIO  
1 = Default

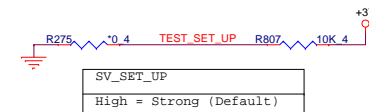


for DS3



Intel ME Crypto Transport Layer  
Security (TLS) cipher suite

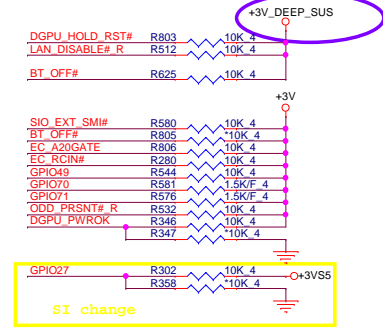
Low = Disable (Default)  
High = Enable



SV\_SET\_UP

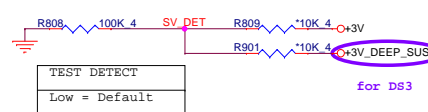
High = Strong (Default)

### GPIO Pull-up/Pull-down(CLG) for DS3



BIOS RECOVERY

High = Disable (Default)  
Low = Enable



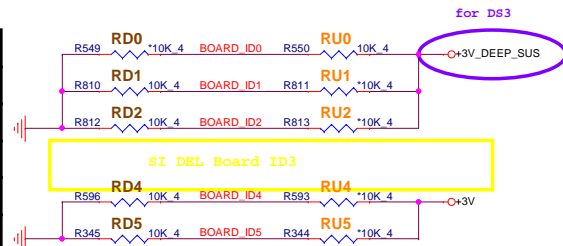
for DS3

### BOARD ID SETTING

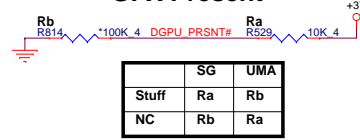
BOARD\_ID1  
For Stage Use

BOARD\_ID0  
BOARD\_ID1  
BOARD\_ID2

| Model      | BOARD_ID5 | BOARD_ID4 | BOARD_ID3 | BOARD_ID2 | BOARD_ID1 | BOARD_ID0 |
|------------|-----------|-----------|-----------|-----------|-----------|-----------|
| DB R62 UMA |           |           | 0         | 0         | 0         | 0         |
| DB R62 DIS |           |           | 0         | 0         | 1         | 1         |
|            |           |           | 0         | 1         | 1         | 1         |
|            |           |           | 0         | 0         | 0         | 0         |



### GFX Present



|       |     |
|-------|-----|
| SG    | UMA |
| Stuff | Ra  |
| NC    | Rb  |

**PROJECT : R62**  
Quanta Computer Inc.

Size Custom

Document Number PCH 4/6 (GPIO/MISC)

Date: Monday, October 22, 2012

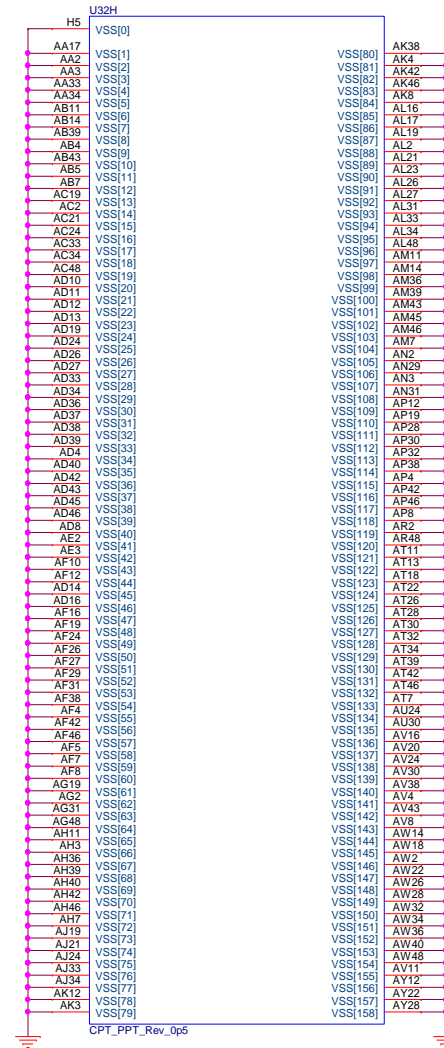
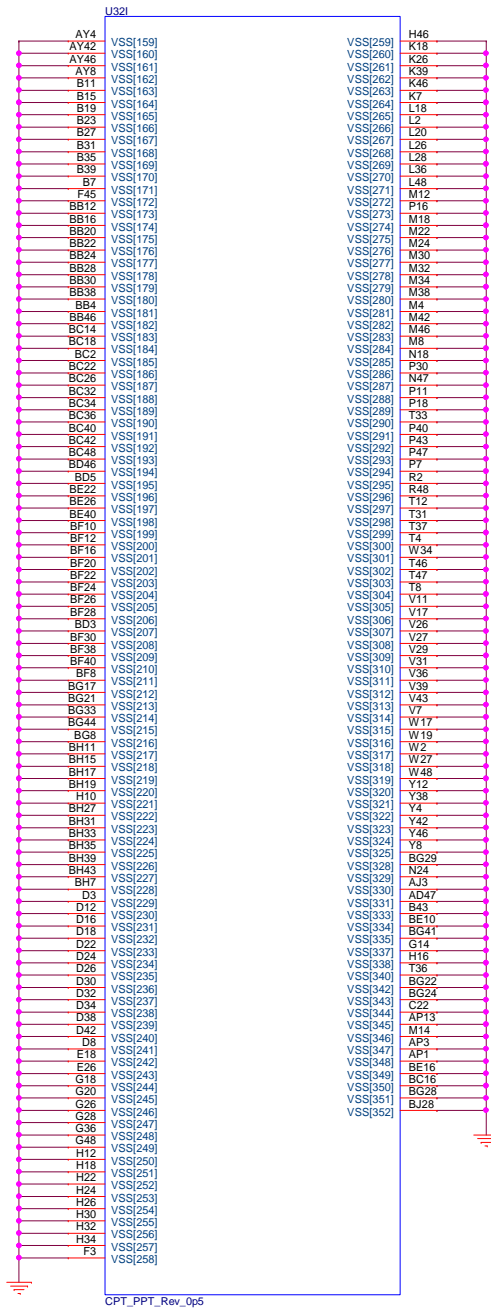
Rev 1A

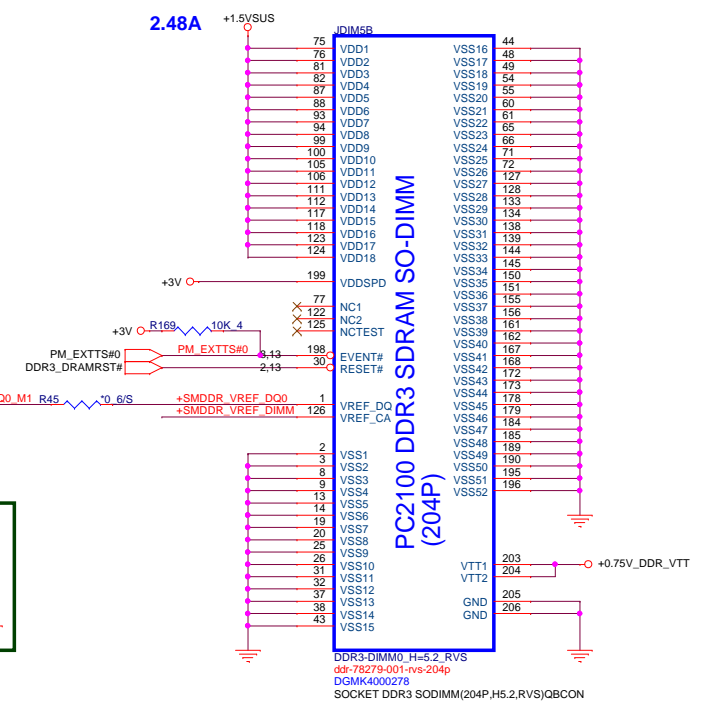
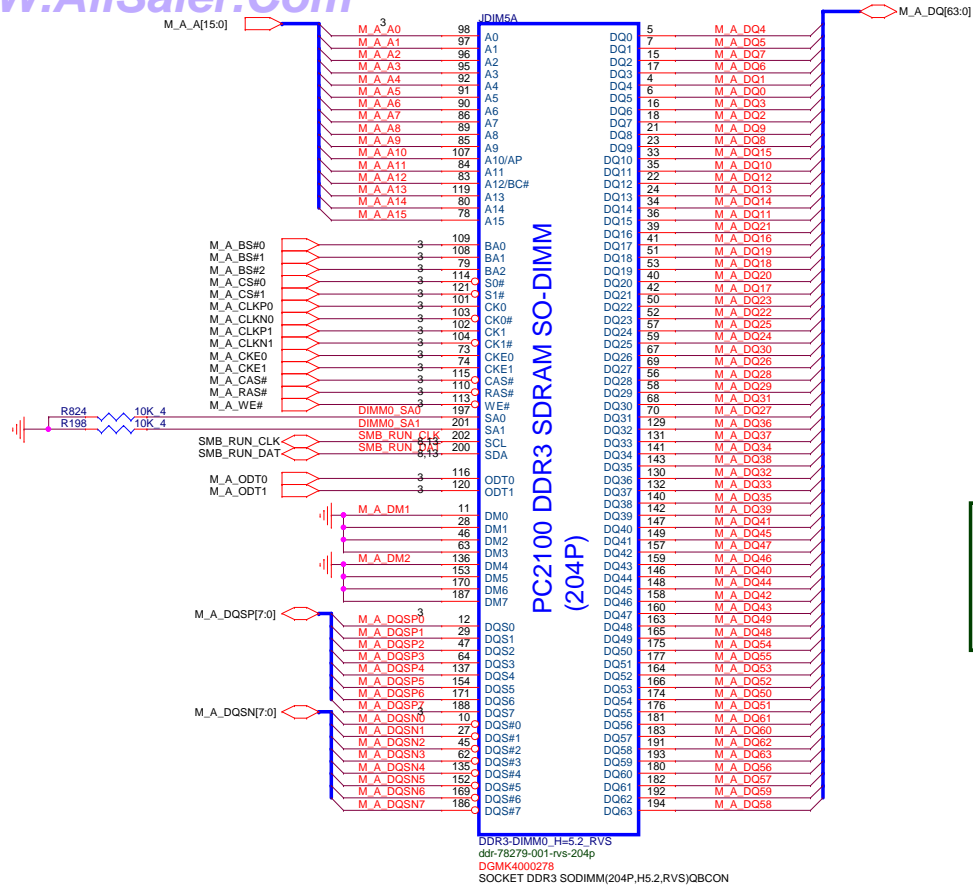
Sheet 9 of 43

## COUGAR POINT/Panther Point (POWER)



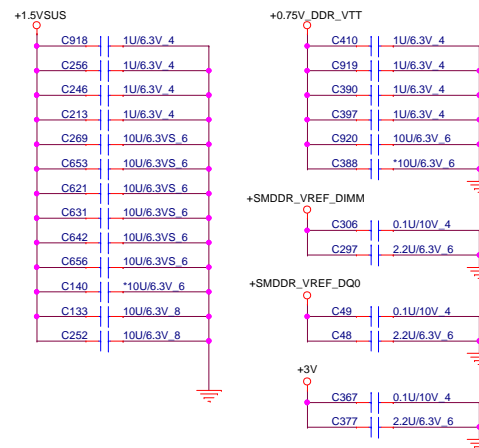




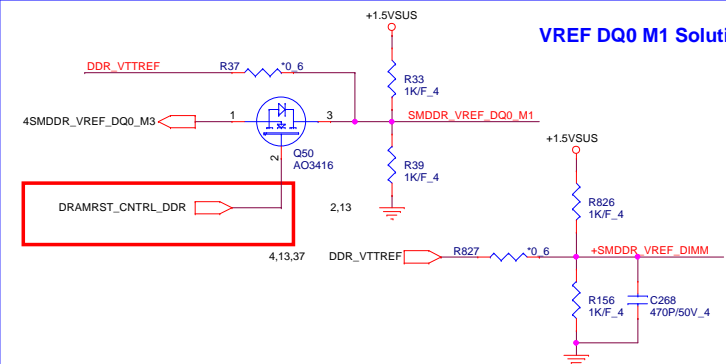


|                |  |
|----------------|--|
| +1.5V          | 4,10,27,33   |
| +0.75V_DDR_VTT | 3,37,39  |
| +1.5VSUS       | 2,4,13,37,43   |
| +3VPCU         | 5,7,25,30,31,33,34,35  |
| +3V            | 2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42 |

## Place these Caps near So-Dimm0.

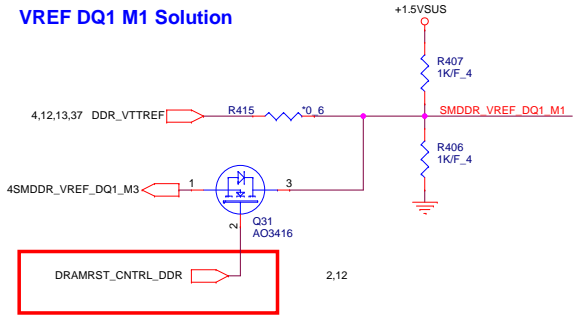
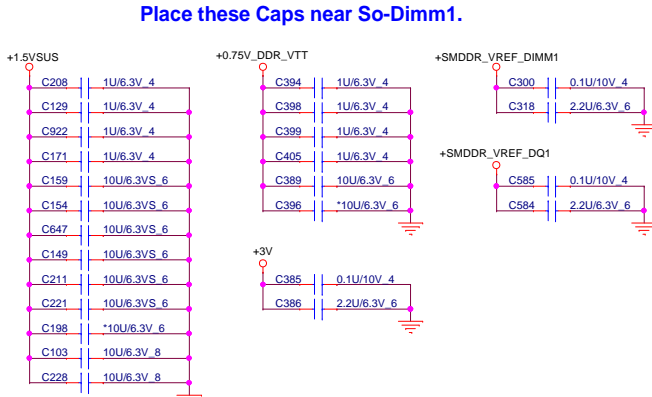
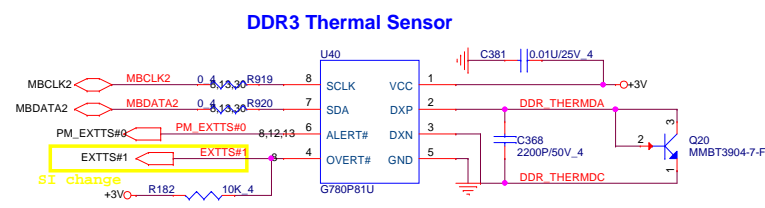
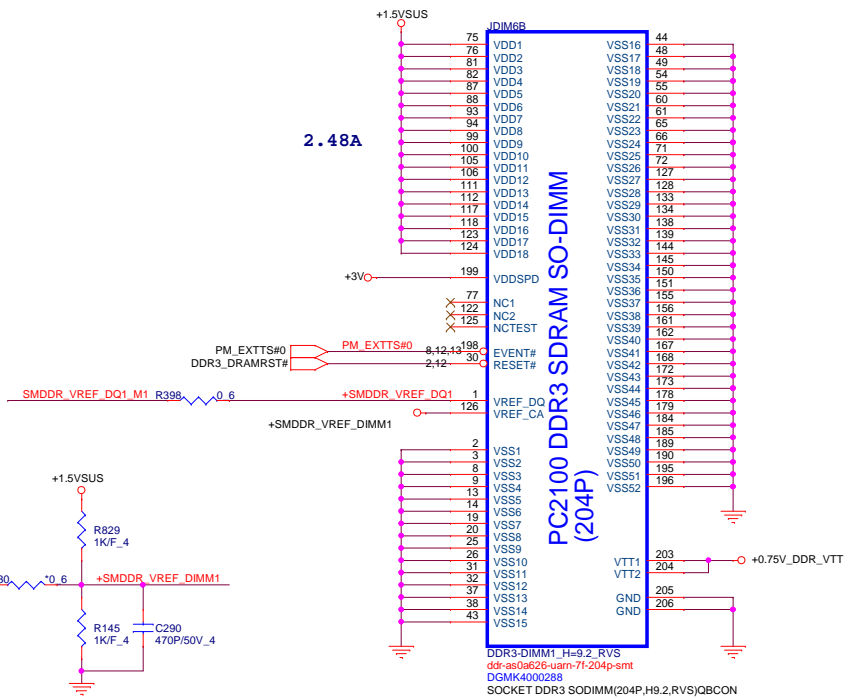


## VREF DQ0 M1 Solution

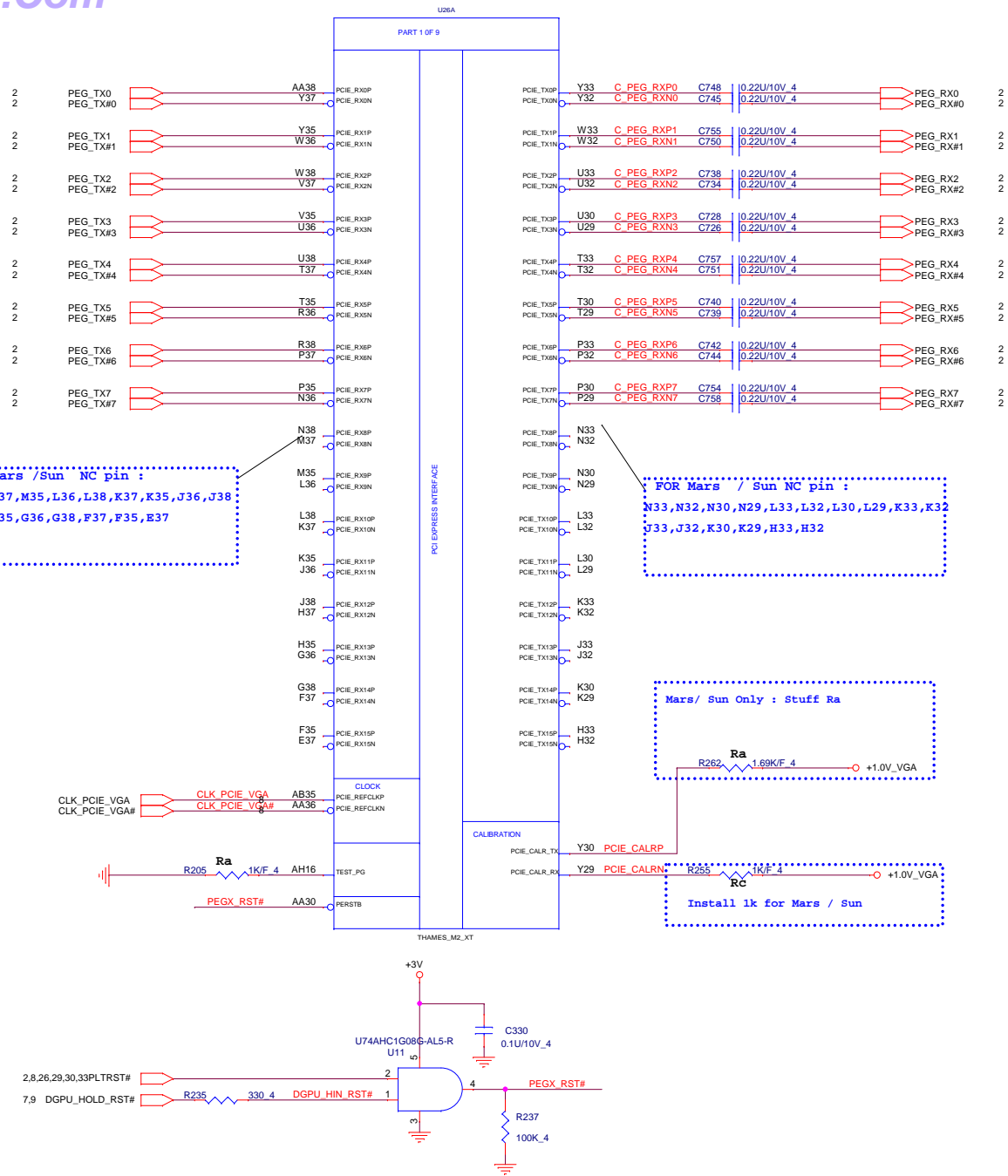


|     |  |  |           |
|-----|--|--|-----------|
| NB5 | <b>PROJECT : R62</b><br>Quanta Computer Inc. |  | Rev<br>1A |
|     | Size<br>Custom                               | Document Number<br>DDR3 DIMM0-RVS (5.2H) |           |
|     | Date: Monday, October 22, 2012               | Sheet 12 of 43                           |           |

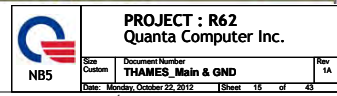




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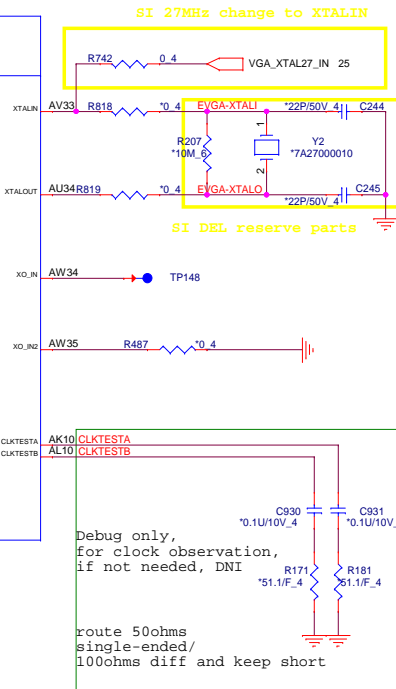
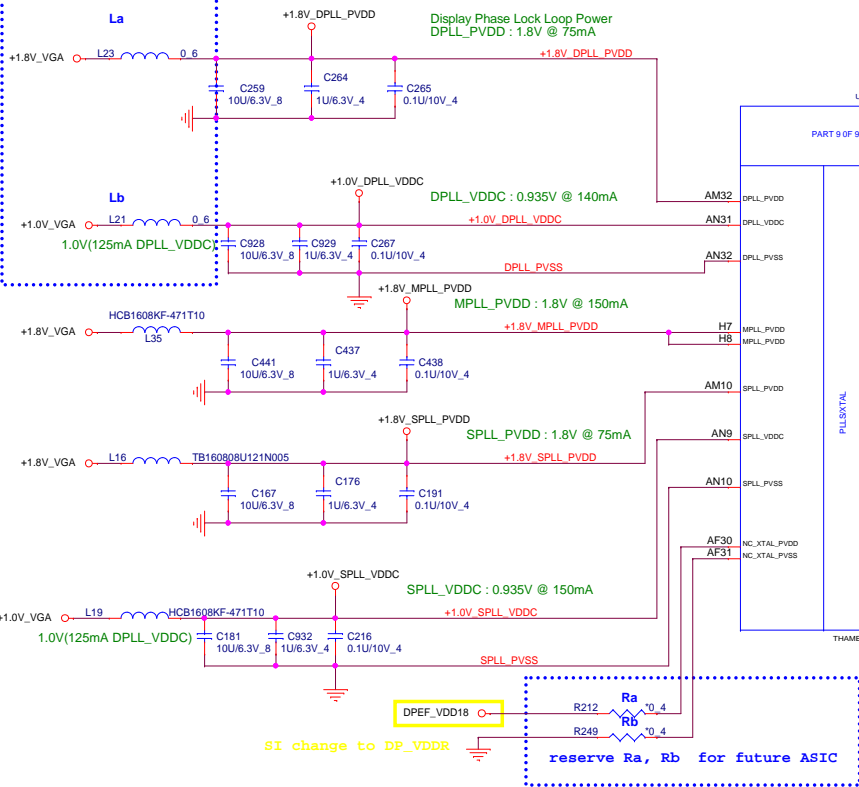




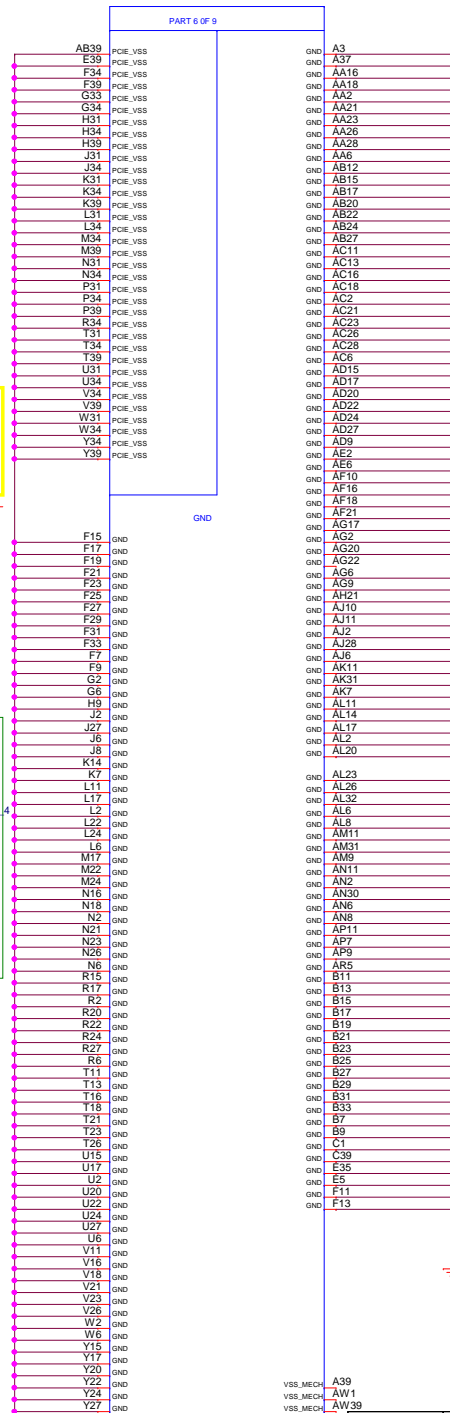


|             |   |
|-------------|---|
| Memory Type |   |
| DDR3        | 27-MHz ( $\pm 30$ ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.   |
| GDDR5       | 27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.) |

For Mars/ Sun  
Change La, Lb  
Bead to 0 ohm



14,18,19,43 +1.0V\_VGA → +1.0V\_VGA  
15,18,19,25,42 +1.8V\_VGA → +1.8V\_VGA

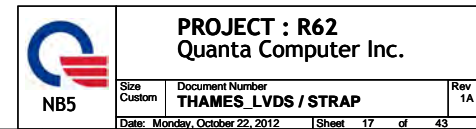


|                                       |                                |           |
|---------------------------------------|--------------------------------|-----------|
| PROJECT : R62<br>Quanta Computer Inc. |                                |           |
| Size<br>Custom                        | Document Number<br>THAMES_XTAL | Rev<br>1A |
| Date: Monday, October 22, 2012        | Sheet 16                       | of 43     |

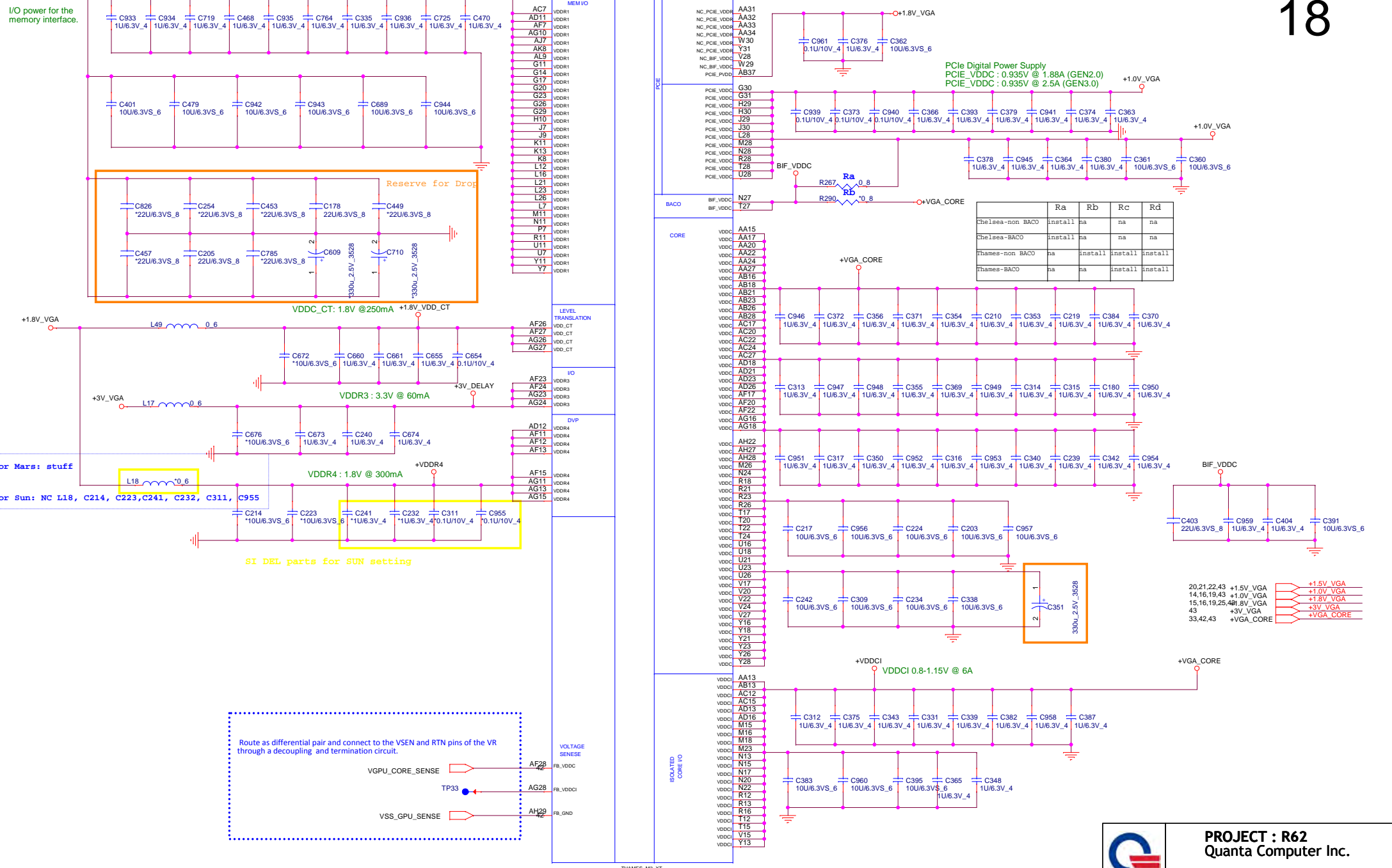


It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

## Power Up/Down Sequence





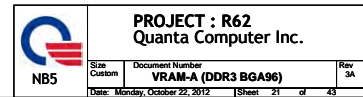




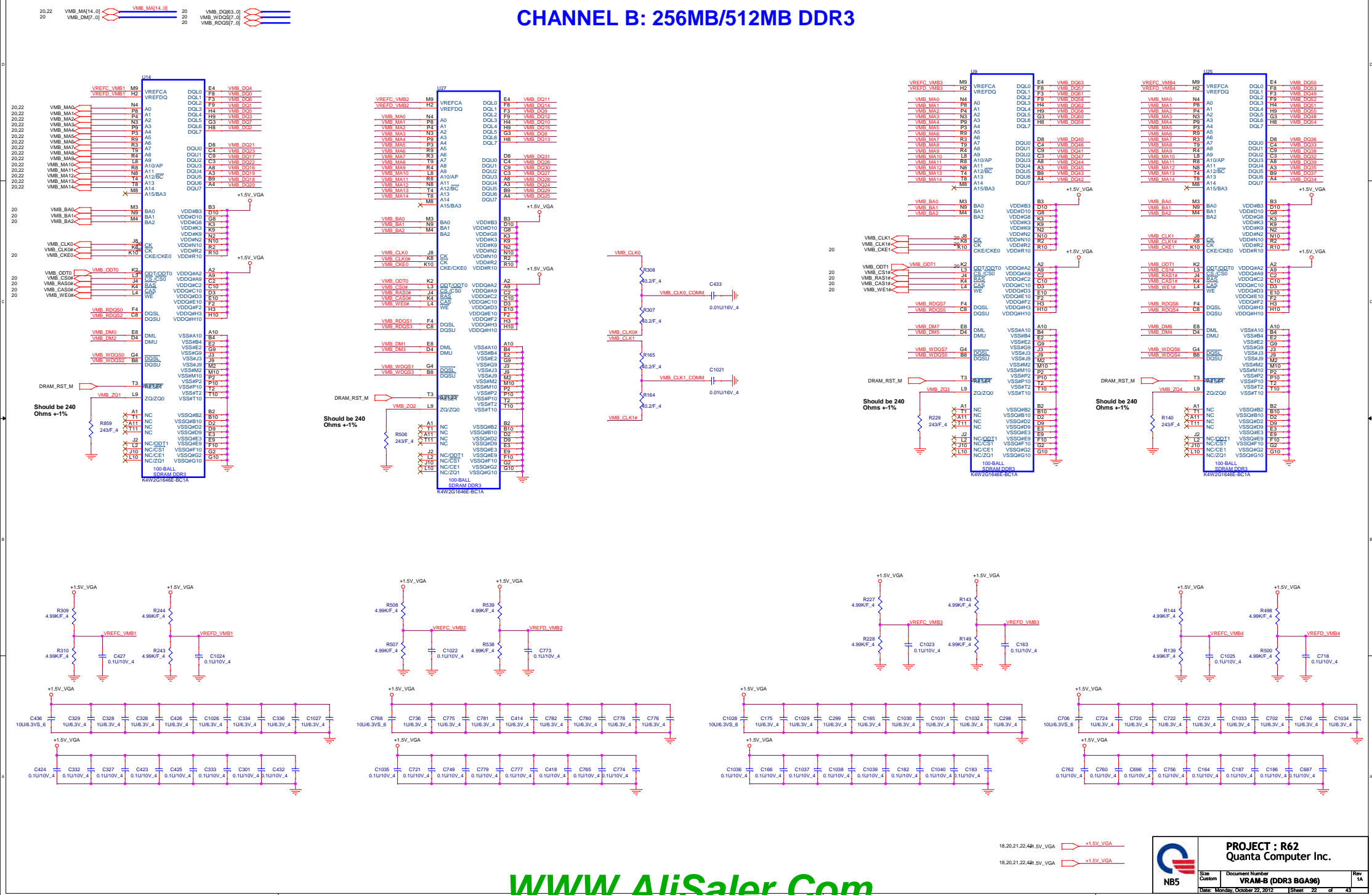


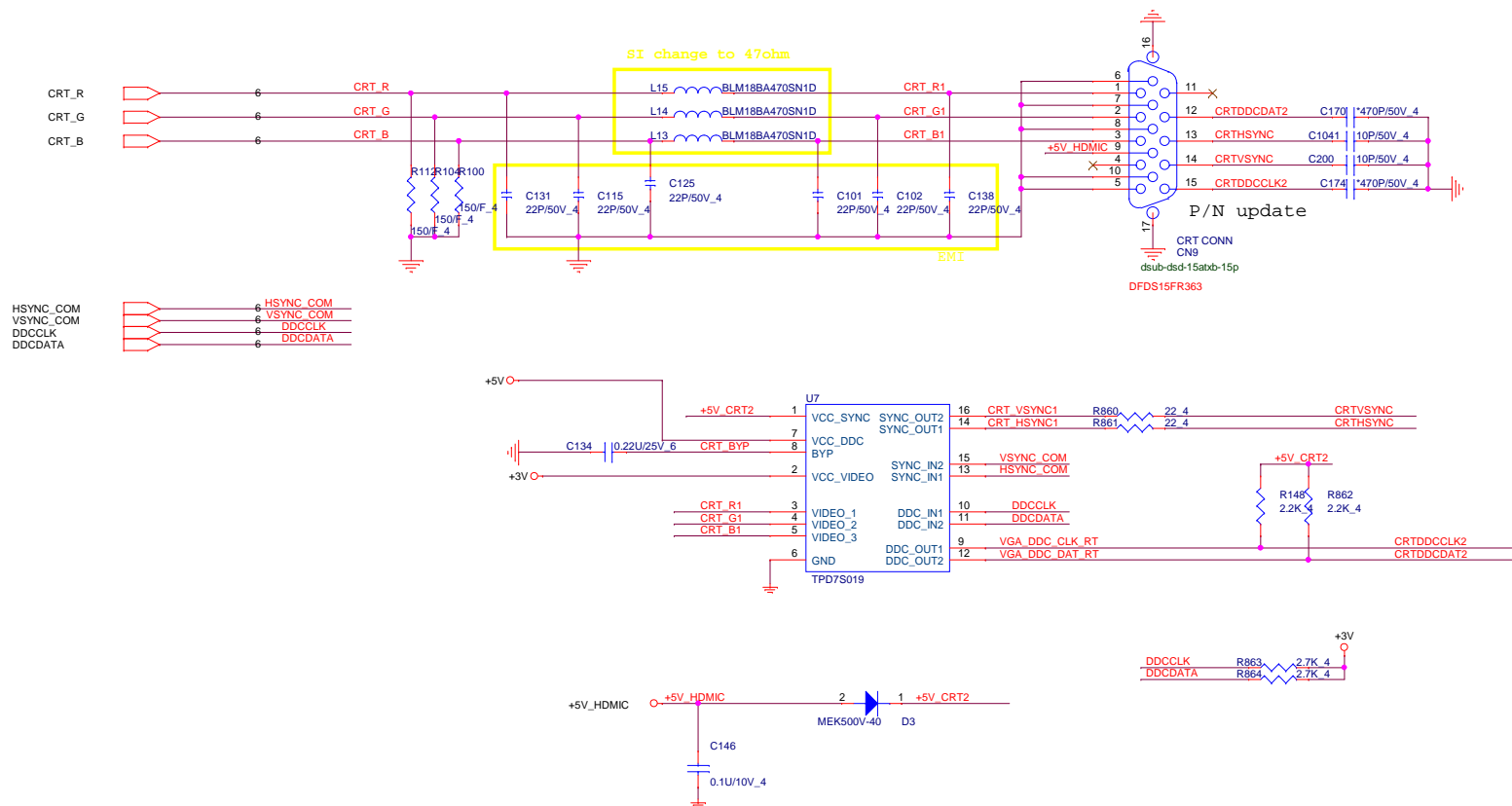


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## CHANNEL B: 256MB/512MB DDR3





# HOLE

## FAN hole

## PCH BKT

## CPU BKT

## VGA BKT

Nut PN:MBBU2005010

## THERMAL BKT

## KB lock

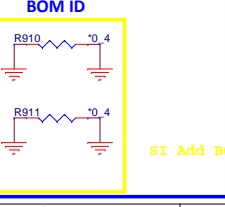
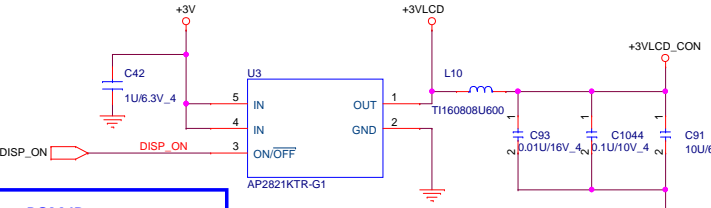
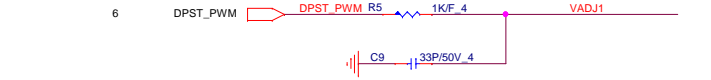
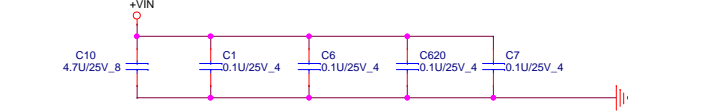
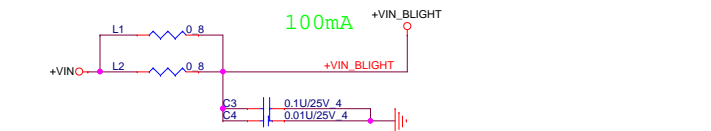
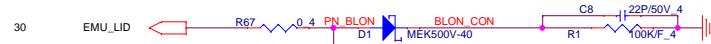
Nut PN:MBUL1001010

SI add EMI PAD

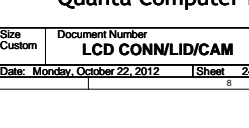
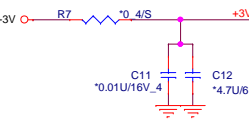
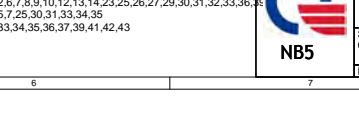
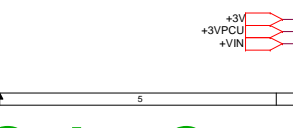
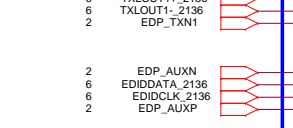
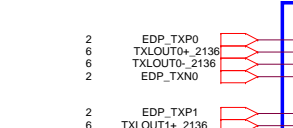
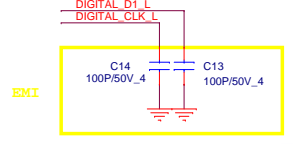
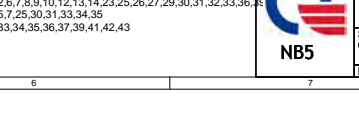
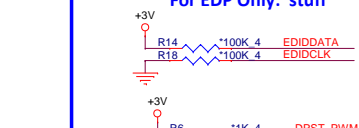
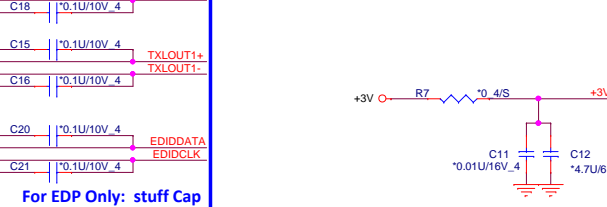
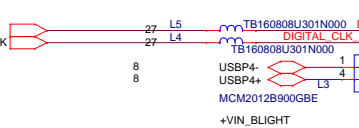
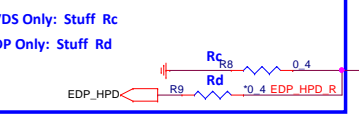
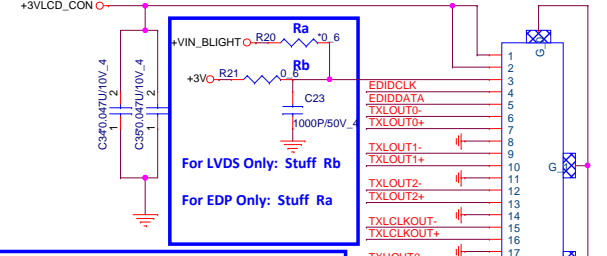
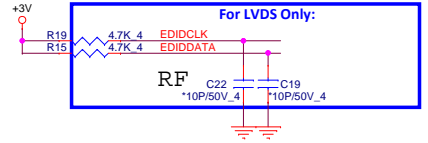
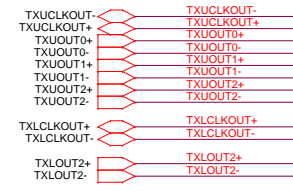
|  |  |                                    |           |
|--|--|------------------------------------|-----------|
|  | <b>PROJECT : R62</b><br>Quanta Computer Inc. |                                    |           |
|  | Size Custom                                  | Document Number<br><b>CRT,Hole</b> | Rev<br>1A |
|  | Date: Monday, October 22, 2012               |                                    |           |



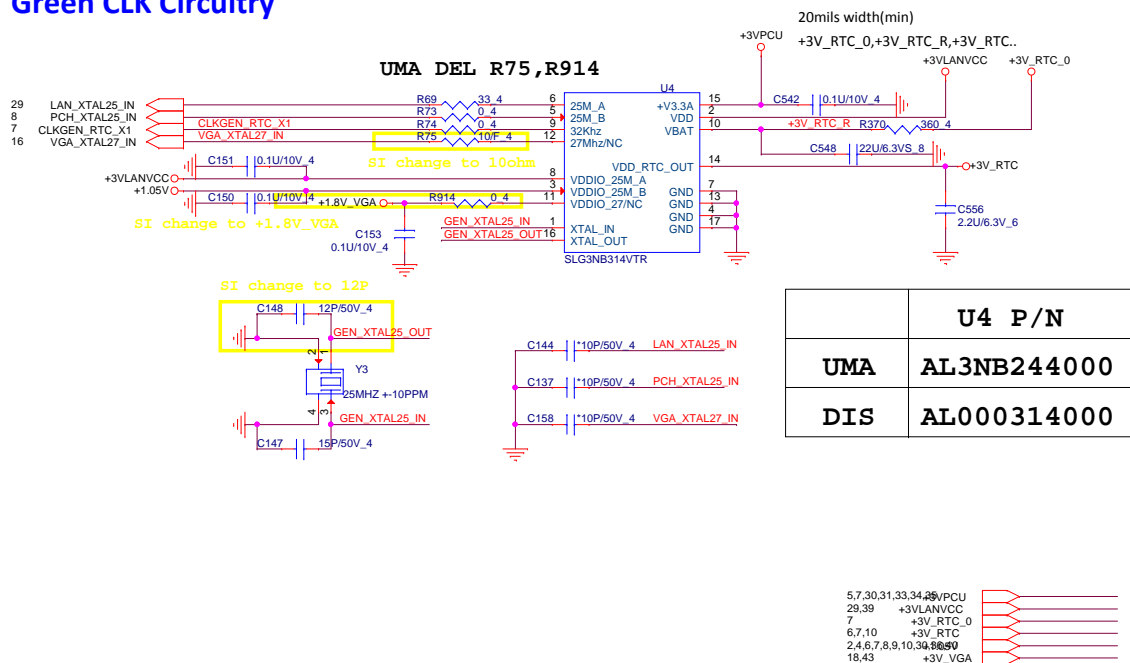
# LID Switch



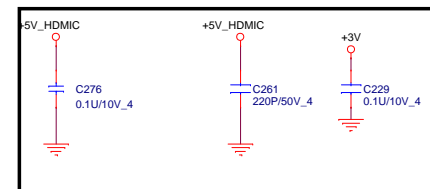
SI Add BOM ID



|                                |                 |                      |       |
|--------------------------------|-----------------|----------------------|-------|
| PROJECT : R62                  |                 | Quanta Computer Inc. |       |
| Size                           | Document Number | LCD CONN/LID/CAM     |       |
| Custom                         | Rev             | 1A                   |       |
| Date: Monday, October 22, 2012 | Sheet           | 24                   | of 43 |

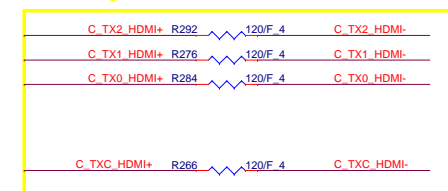


EMI request



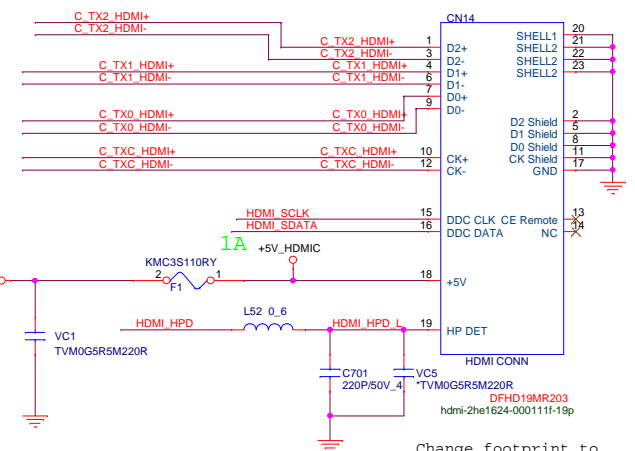
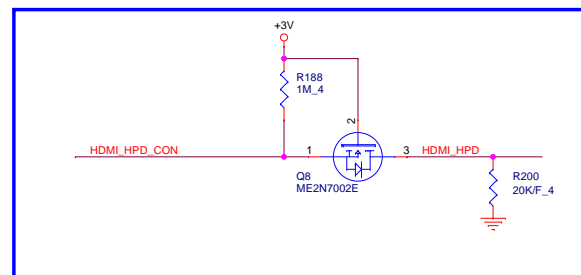
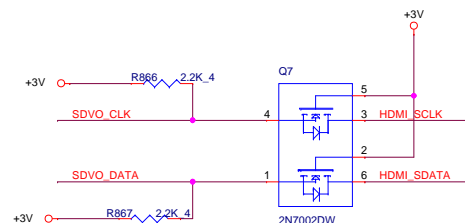
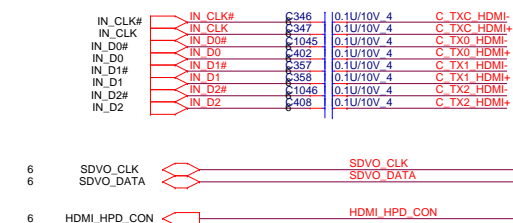
7,10,23,27,31,32,33,34,35V  
23 +5V\_HDMIC  
2,6,7,8,9,10,12,13,14,23,24,26,27,29,30,31,32,33,36,39,40,42

EMI request

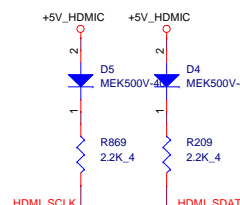


close to HDMI conn

Close to HDMI Connector



Change footprint to  
hdmi-2he1624-000111f-19p



**PROJECT : R62**  
**Quanta Computer Inc.**

Size Custom Document Number **HDMI CONN** Rev 1A

Date: Monday, October 22, 2012 Sheet 25 of 43

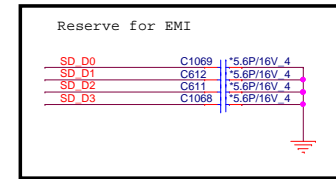
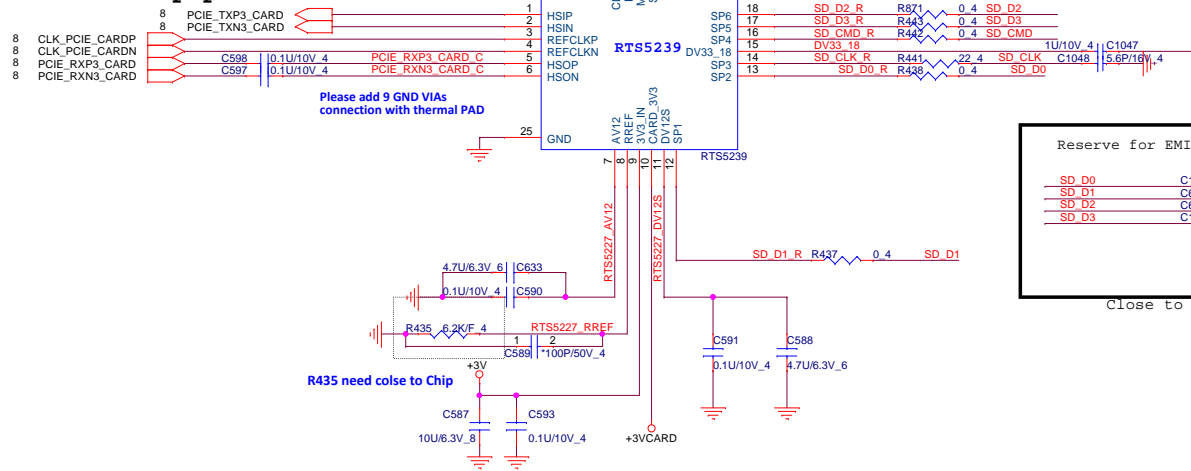
8 CLK\_PCIE\_REQ2# CLK\_PCIE\_REQ2# R446 0.4/S CLK\_PCIE\_REQ2#\_R

|     |        |        |
|-----|--------|--------|
| SP1 | SD D1  | MS D1  |
| SP2 | SD D0  | MS D0  |
| SP3 | SD CLK | MS D0  |
| SP4 | SD CMD | MS D2  |
| SP5 | SD D3  | MS D3  |
| SP6 | SD D2  | MS CLK |
| SP7 | SD_WP  | MS_BS  |

Share Pin

Close to chip pin

Close to chip pin

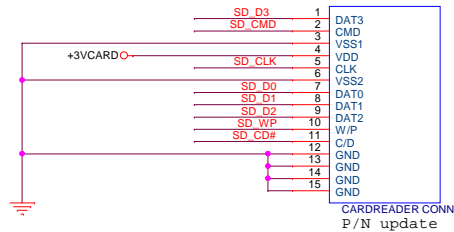


Close to U38

SD / MMC

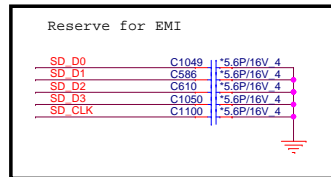
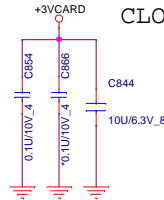
CARD READER

CN8



CARDREADER CONN  
P/N update

CLOSE CONN

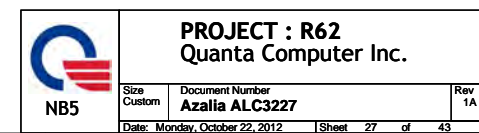


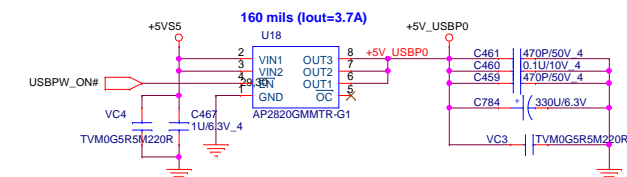
Close to CN8

2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42

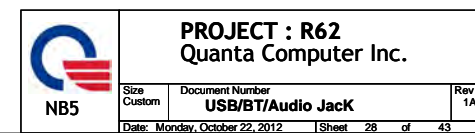
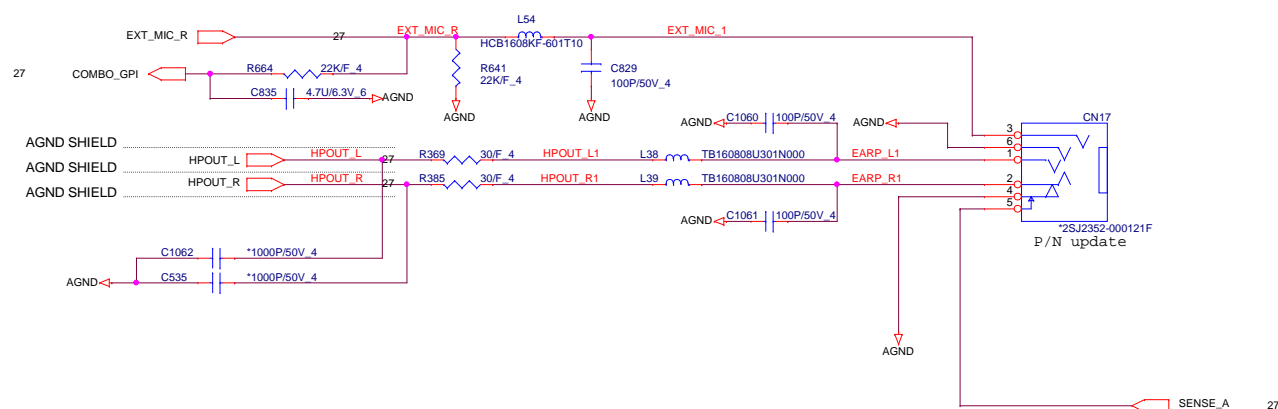
|  |                                       |  |           |
|--|---------------------------------------|--|-----------|
|  | PROJECT : R62<br>Quanta Computer Inc. |  |           |
|  | Size<br>Custom                        | Document Number<br>RTS5229 & CR SOCKET | Rev<br>1A |
|  | Date: Monday, October 22, 2012        | Sheet 26                               | of 43     |

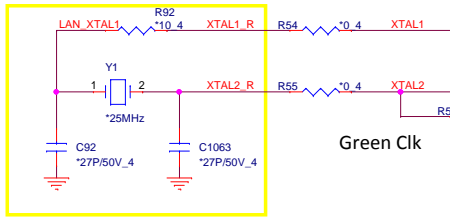






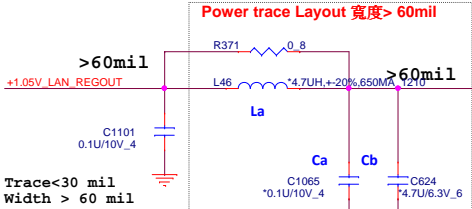
10,29,33,35,36,37,38,39,40,41,42,43  
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42  
25,29,39 +3VLANVCC





For GbE  
\* Place Cc,Cd,Ce,Cf  
close to each VDD10 pin-- 3, 22, 8, 30

For 10/100 NA Ce,Cf  
\* Place Ce, Cf  
close to each VDD10 pin-- 8, 30 only,



For GbE  
Stuff La, Ca, Cb

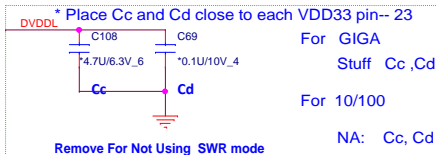
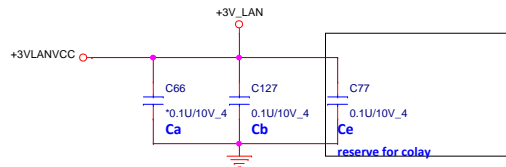
For 10/100  
NA: La, Ca, Cb

For GbE  
\* Place Cf close to each VDD10 pin-- 22 (reserve)

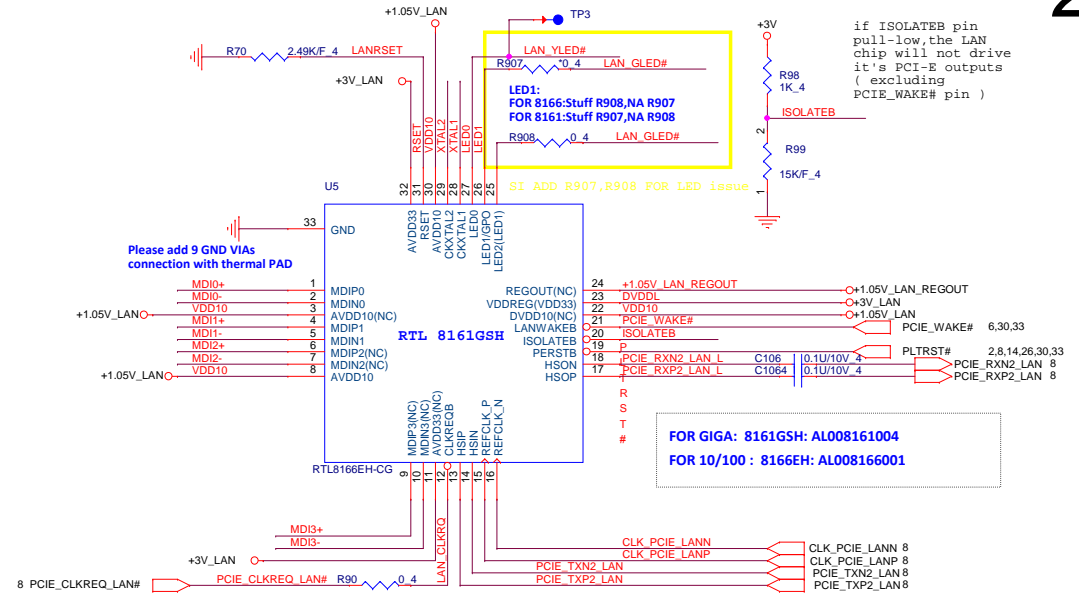
For 10/100  
\* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100  
\* Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32

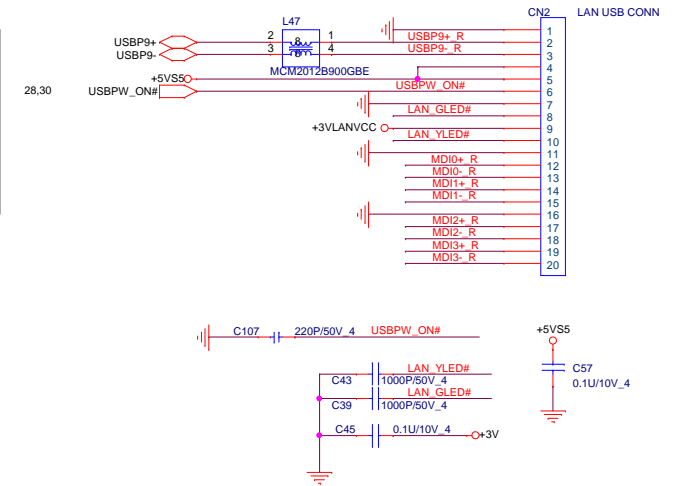
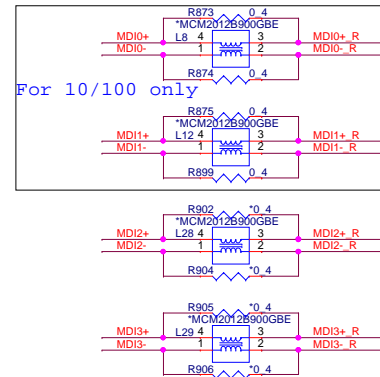
For GIGA  
\* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



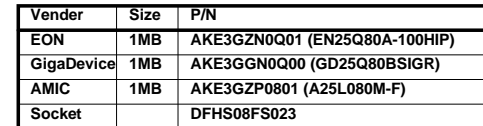
2,6,7,8,9,10,12,13,14,23,24,25,26,27,30,31,32,33,36,39,40,42  
25,39 +3VLANVCC



## Right SIDE USBX1 and LAN CONN



|     |                                       |                                   |           |
|-----|---------------------------------------|-----------------------------------|-----------|
| NB5 | PROJECT : R62<br>Quanta Computer Inc. |                                   |           |
|     | Size<br>Custom                        | Document Number<br>RTL 8105E/RJ45 | Rev<br>1A |
|     | Date: Monday, October 22, 2012        | Sheet 29                          | of 43     |
|     |                                       |                                   |           |



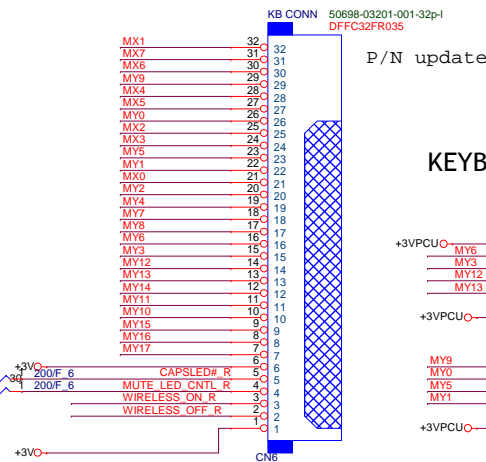
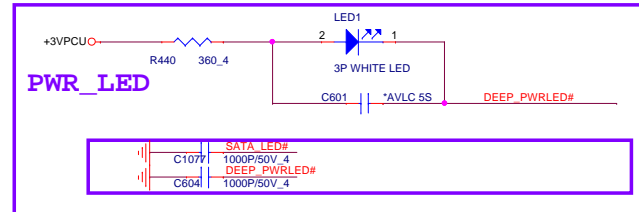
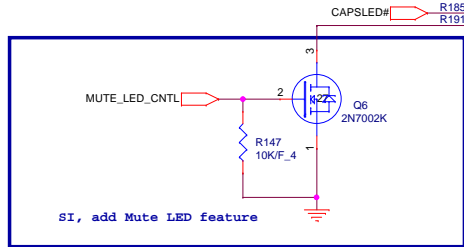
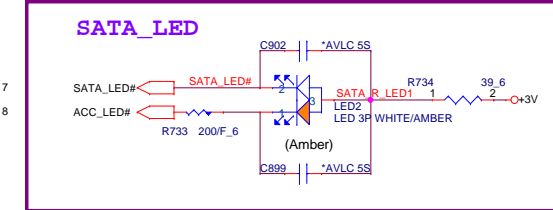
|           |      |     |              |   |
|-----------|------|-----|--------------|---|
| SC1I#     | R887 | 0 4 | SIO_EXT_SCI# | 7 |
| DNBSWON#1 | R286 | 0 4 | DNBSWON#     | 6 |
| KBSMI#1   | R504 | 0 4 | SIO_EXT_SMI# | 9 |



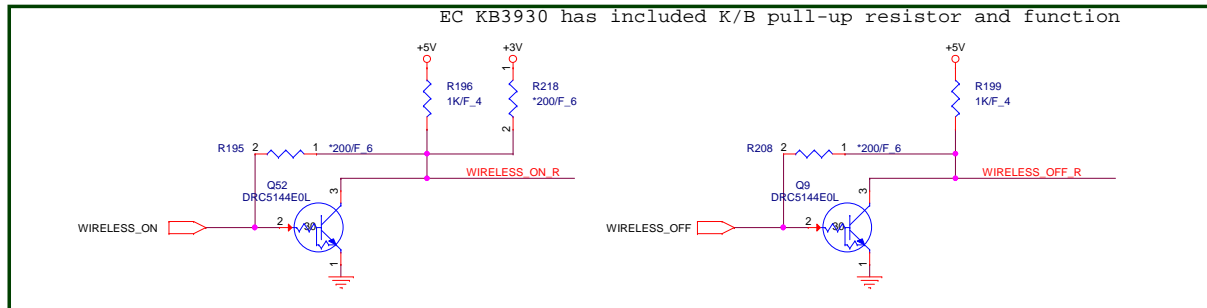
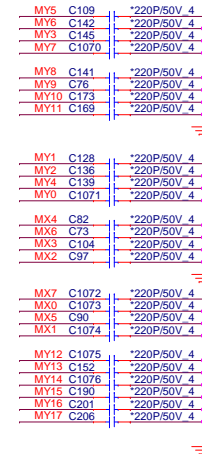
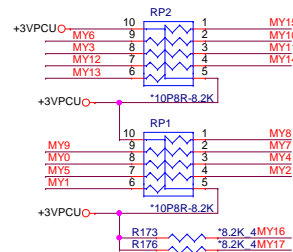
**PROJECT : R62**  
**Quanta Computer Inc.**

|                                |  |                |
|--------------------------------|--|----------------|
| Size<br>Custom                 | Document Number<br><b>EC (KB3940 A1) ROM</b> | Rev<br>1A      |
| Date: Monday, October 22, 2012 |  | Sheet 30 of 43 |

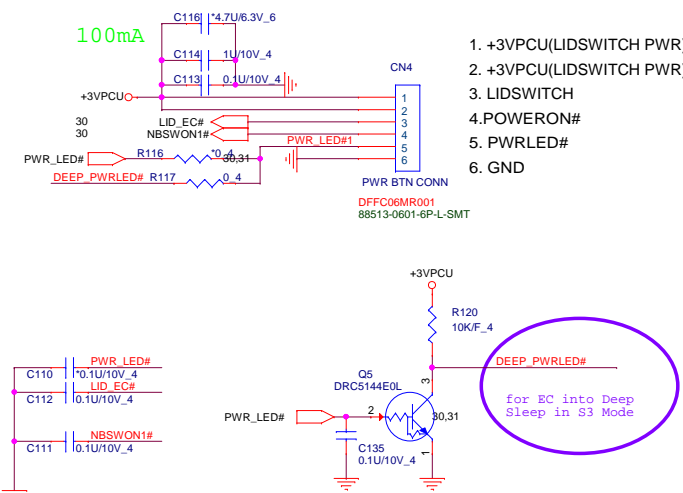




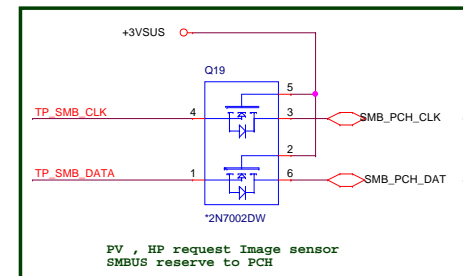
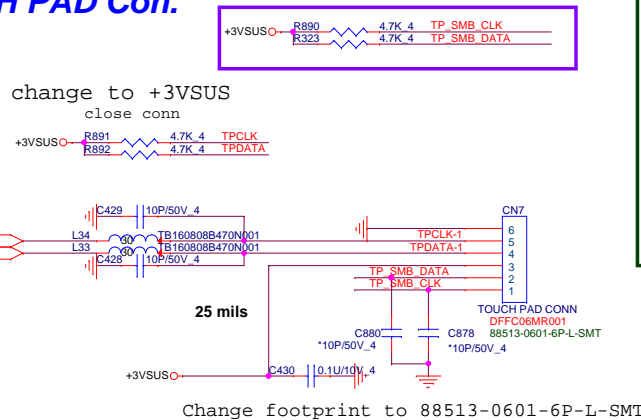
## KEYBOARD PULL-UP



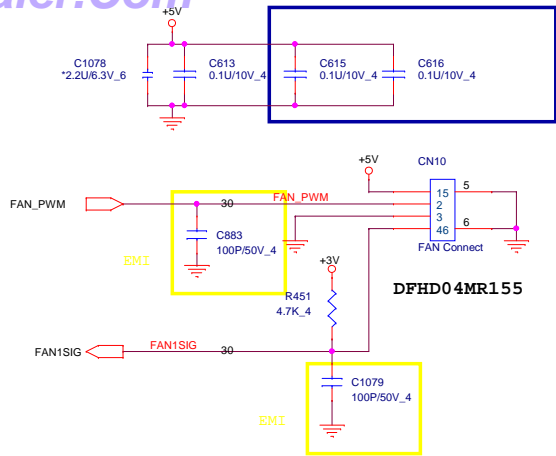
## POWER BOTTON CONNECT



## TOUCH PAD Con.

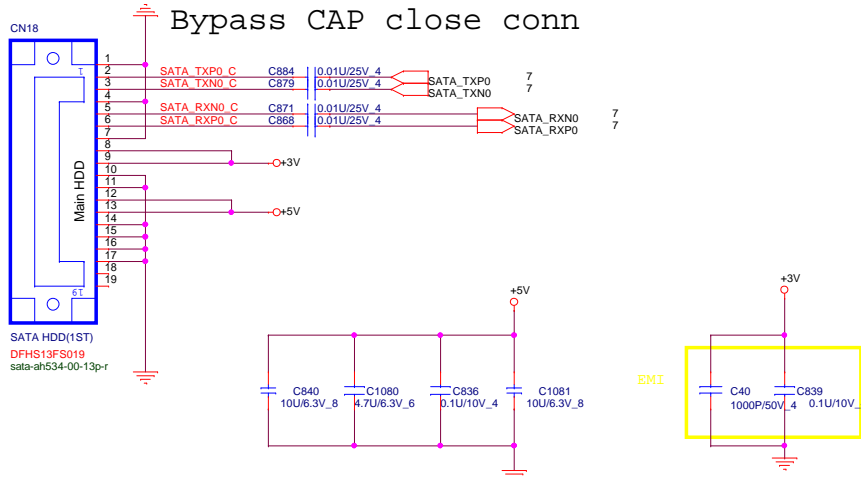


# CPU FAN

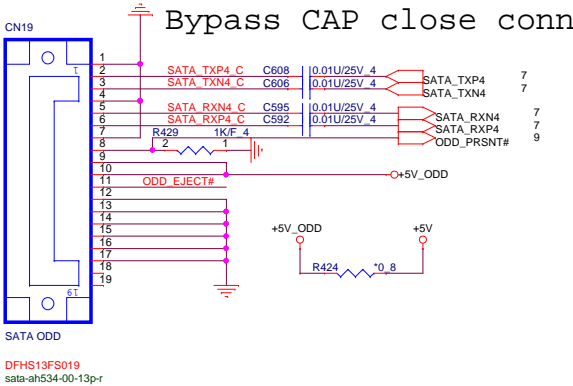


# SATA HDD CONNECTOR

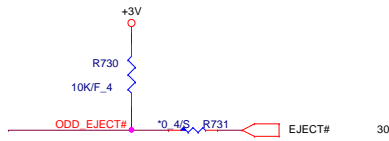
32



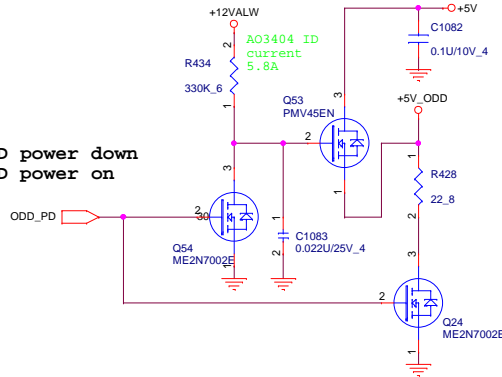
# SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



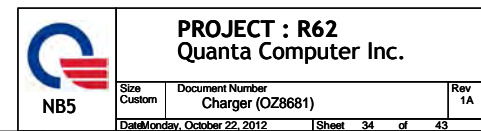
High : ODD power down  
Low : ODD power on



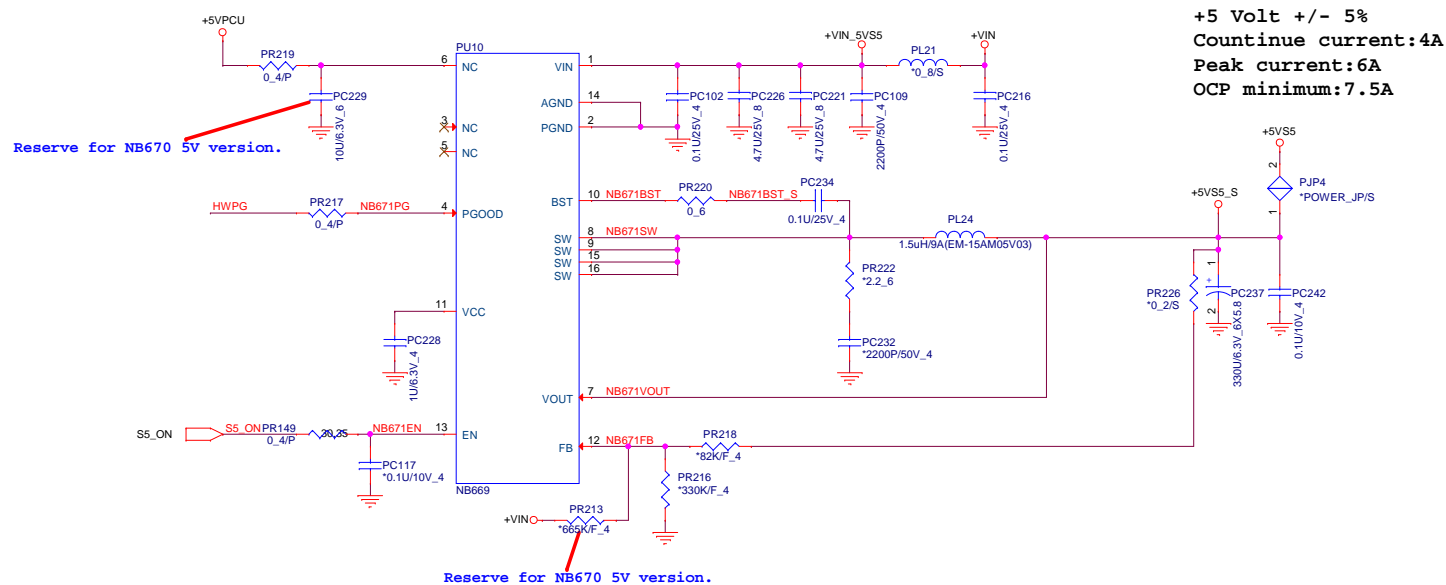
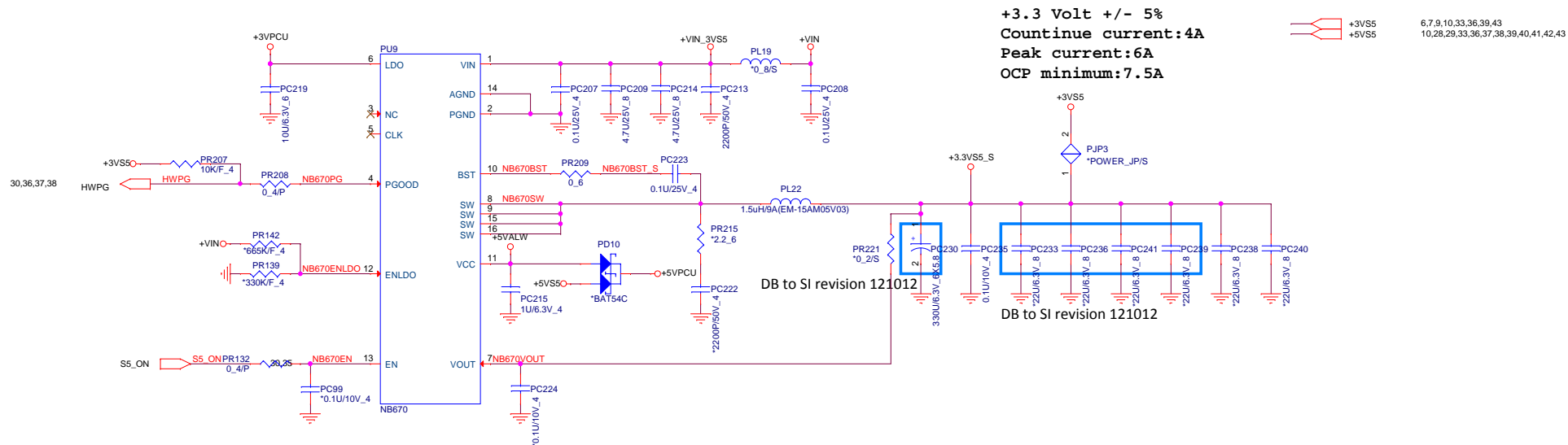
+3V  
+3VPCU  
+5V  
+12VALW  
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42  
5,7,25,30,31,33,34,35  
7,10,23,25,27,31,33,39  
34,39,43

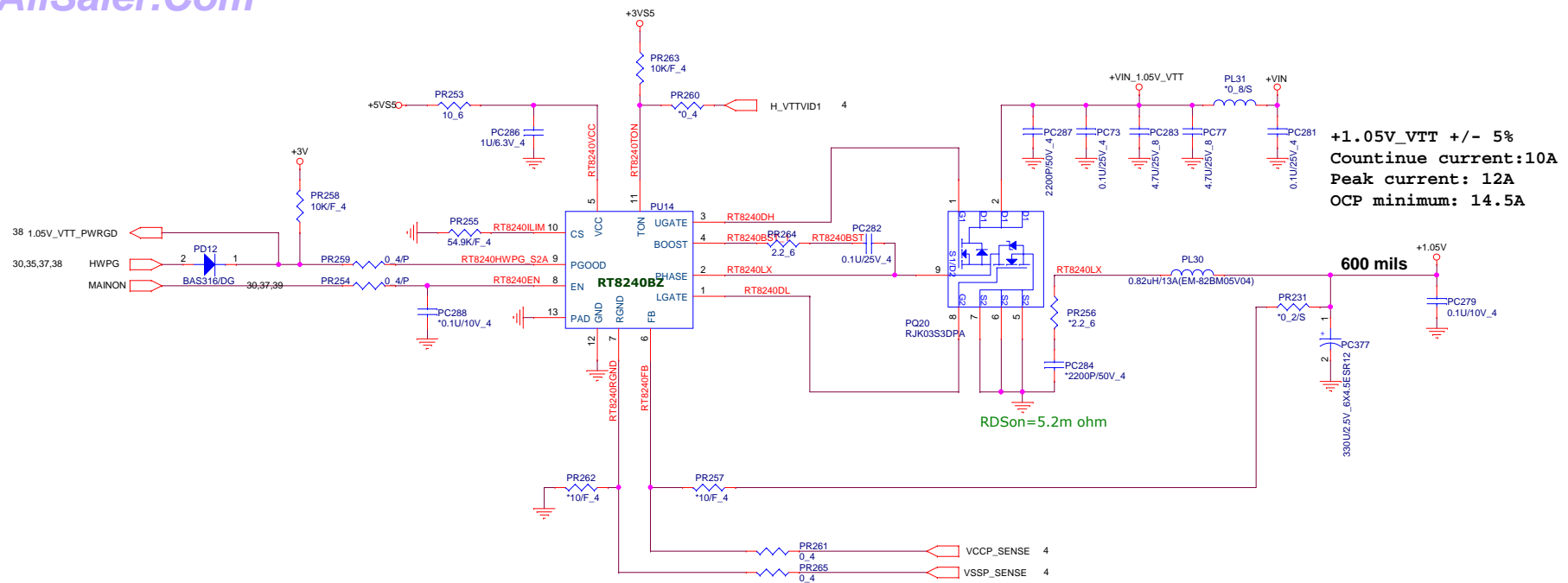
|  |                                       |                                |           |
|--|---------------------------------------|--------------------------------|-----------|
|  | PROJECT : R62<br>Quanta Computer Inc. |                                |           |
|  | Size<br>Custom                        | Document Number<br>HDD/ODD/FAN | Rev<br>1A |
|  | Date: Monday, October 22, 2012        | Sheet 32                       | of 43     |

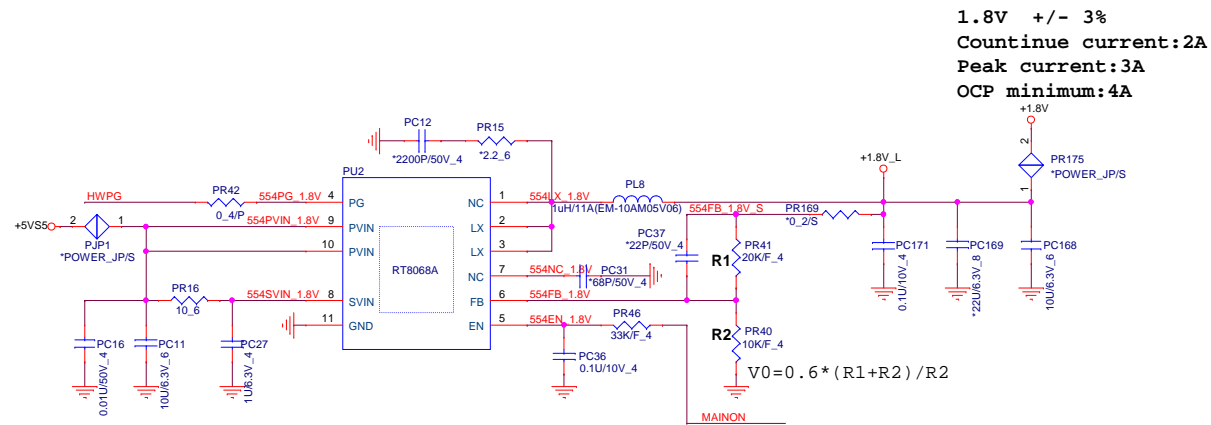
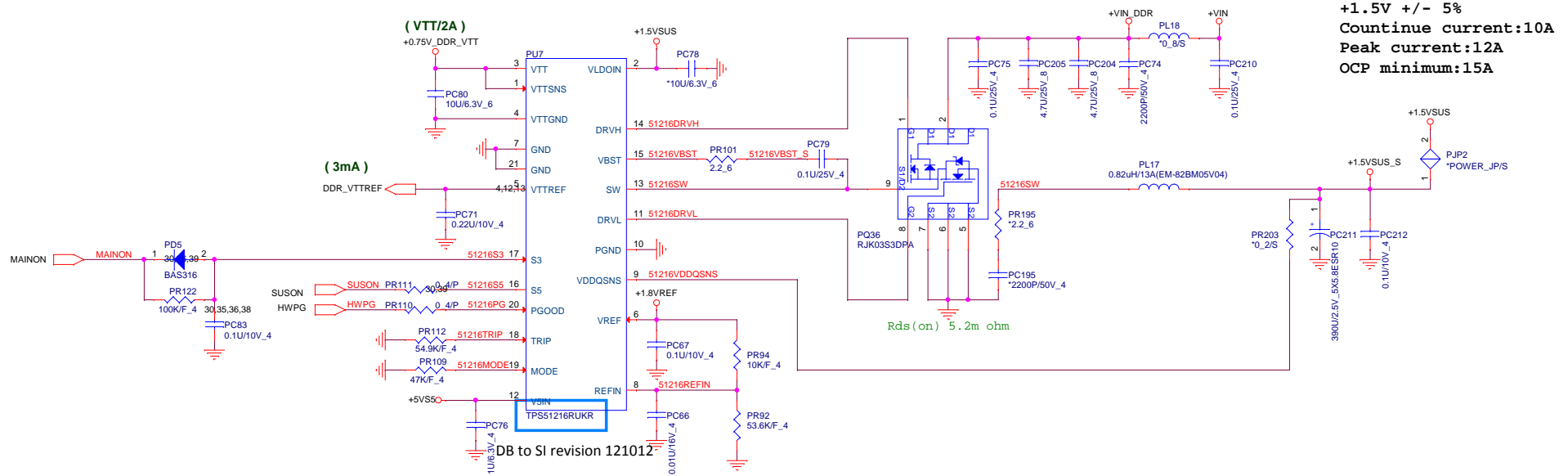








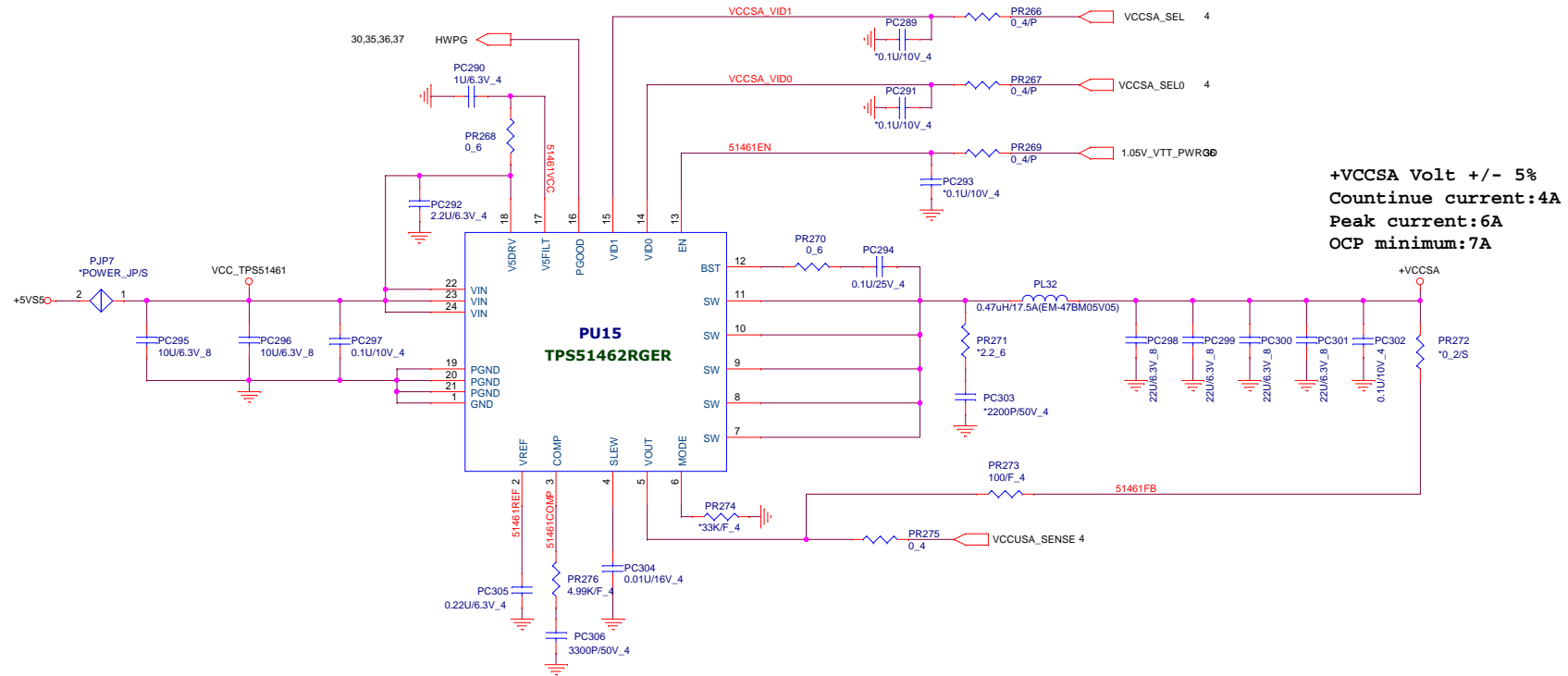




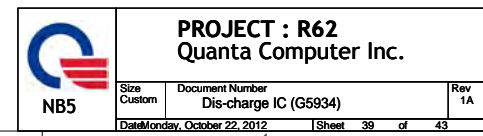
**TPSS1462RGER/AL051462000**

For CPU SV system agent  
voltage slew rate of 0.5 -10 mV/μs

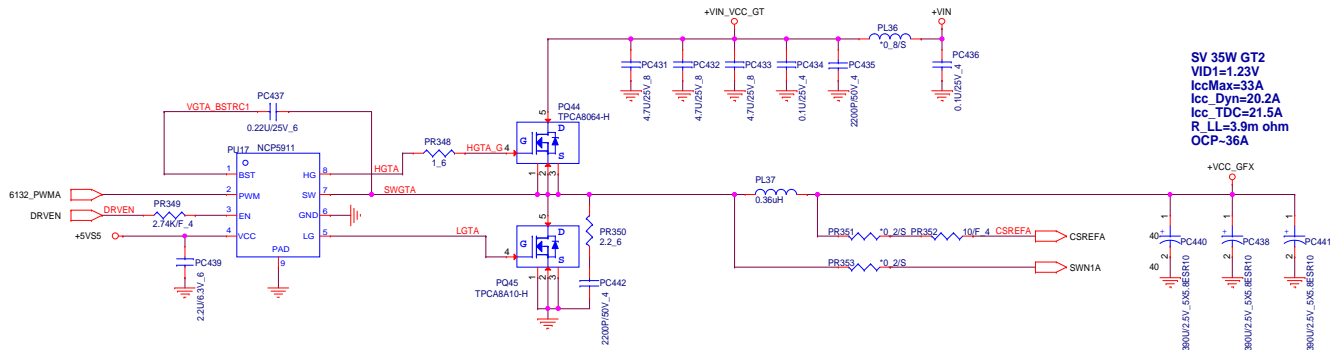
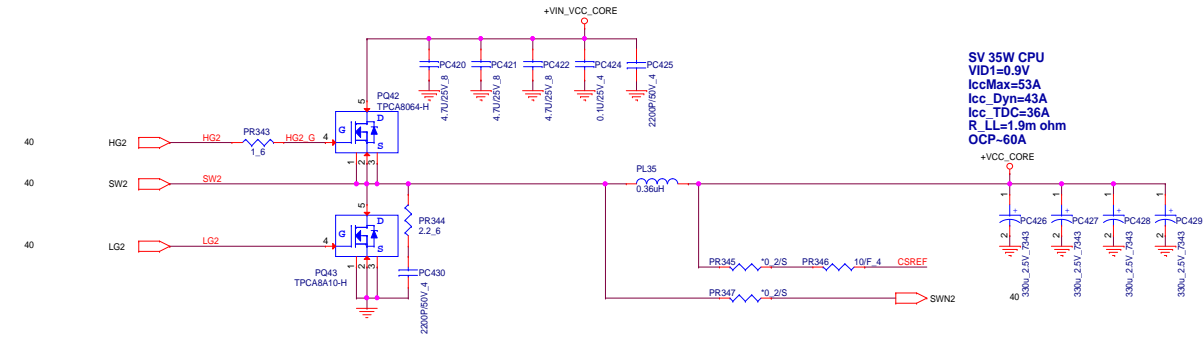
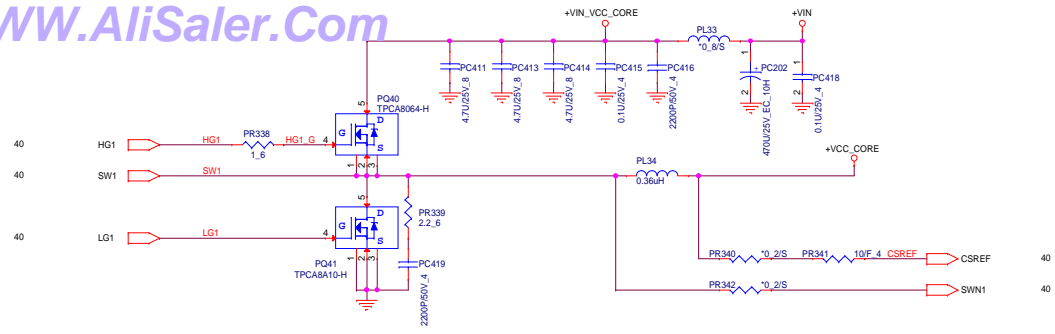
| SEL0 | SEL1 | +VCCSA |
|------|------|--------|
| 0    | 0    | 0.9V   |
| 0    | 1    | 0.8V   |
| 1    | 0    | 0.725V |
| 1    | 1    | 0.675V |





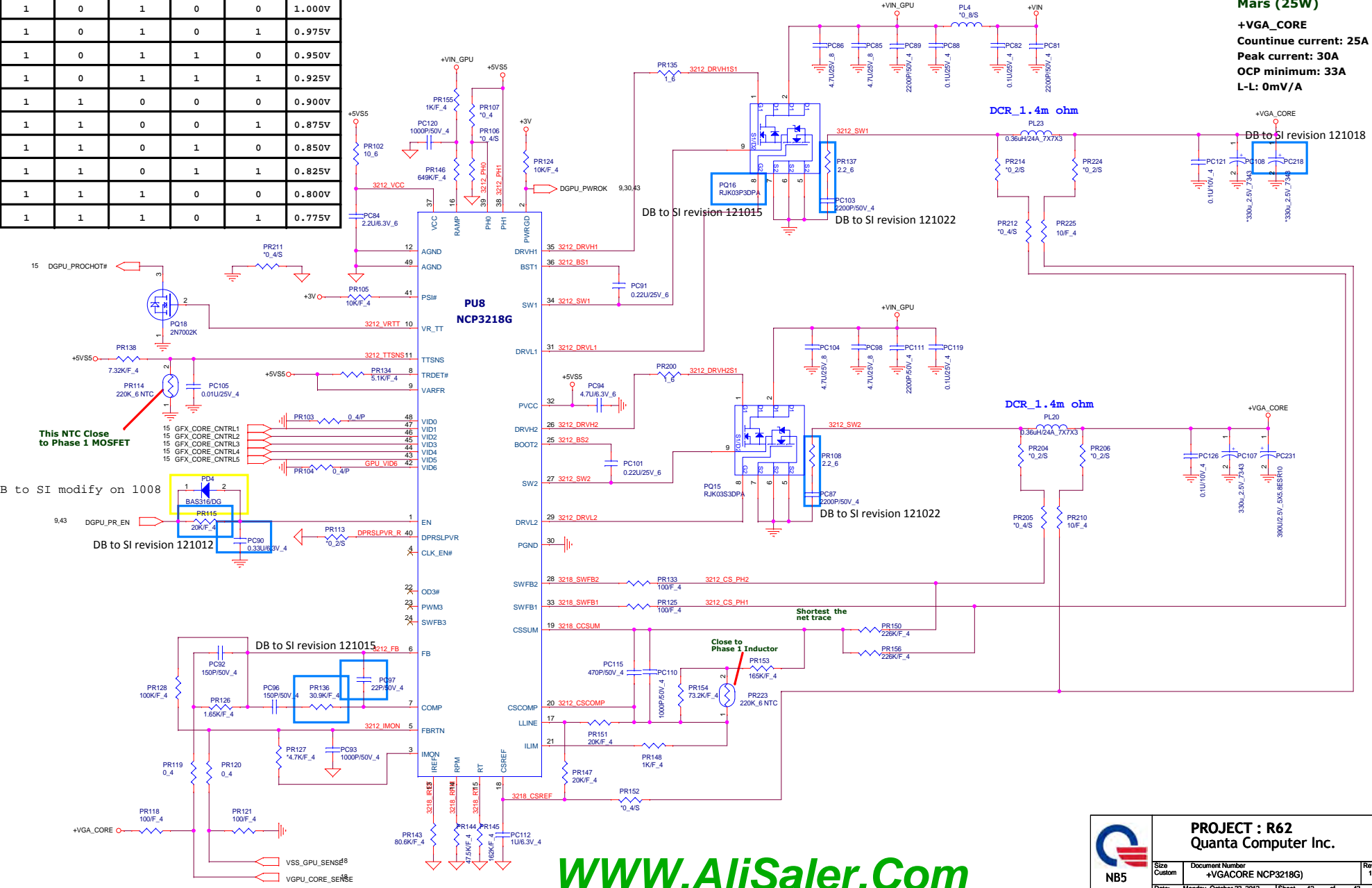






| PWRCNTL5 | PWRCNTL4 | PWRCNTL3 | PWRCNTL2 | PWRCNTL1 | V-CORE |
|----------|----------|----------|----------|----------|--------|
| 0        | 1        | 1        | 1        | 1        | 1.125V |
| 1        | 0        | 0        | 0        | 0        | 1.100V |
| 1        | 0        | 0        | 0        | 1        | 1.075V |
| 1        | 0        | 0        | 1        | 0        | 1.050V |
| 1        | 0        | 0        | 1        | 1        | 1.025V |
| 1        | 0        | 1        | 0        | 0        | 1.000V |
| 1        | 0        | 1        | 0        | 1        | 0.975V |
| 1        | 0        | 1        | 1        | 0        | 0.950V |
| 1        | 0        | 1        | 1        | 1        | 0.925V |
| 1        | 1        | 0        | 0        | 0        | 0.900V |
| 1        | 1        | 0        | 0        | 1        | 0.875V |
| 1        | 1        | 0        | 1        | 0        | 0.850V |
| 1        | 1        | 0        | 1        | 1        | 0.825V |
| 1        | 1        | 1        | 0        | 0        | 0.800V |
| 1        | 1        | 1        | 0        | 1        | 0.775V |

Default



**Mars (25W)**  
**+VGA\_CORE**  
Countinue current: 25A  
Peak current: 30A  
OCP minimum: 33A  
L-L: 0mV/A



+0.95V +/- 3%  
Continue current:2A  
Peak current:3A  
OCP minimum:4A

